

APPLICATION NOTE

**Application information for
TDA8358J N2
deflection output circuit with
East - West amplifier**

AN10114-01

Version 1.0
June 2002



ABSTRACT

This report gives a description of the TDA8358JN1 version with a description of the TDA8358JN2 version together with application aspects.

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APPLICATION NOTE

Application information for TDA8358JN2 deflection output circuit with East - West amplifier AN10114-01

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East - West amplifier
Robust against flashover
90°, 110°

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Summary

In this report you can find an application and product description of the DC coupled deflection output circuit with the type number TDA8358J. The TDA8358J is functional the same as the TDA8359J, but the TDA8358J has an additional east -west amplifier. A description is given of the differences between the TDA8358JN1 and TDA8358JN2. The application design procedure and the application investigations are given at the end of this report.

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1. INTRODUCTION.

The TDA8358J is an integrated power circuit for use in 90° and 110° colour deflection systems. It contains a vertical deflection bridge output, which operates as a high efficiency class G system and can handle field frequencies from 25 to 200 Hz. The vertical deflection coil of a 4 : 3 as well a 16 : 9 picture tube can be connected to this vertical deflection device. Due to the bridge configuration a DC deflection output application can be designed with a single positive main supply of typical 12-Volt and a positive flyback supply of typical 45-Volt. (Depending on the vertical deflection coil data). The input configuration is symmetrical in order to have improved EMI behaviour.

The integrated circuit is designed in a Low Voltage DMOS (LVDMOS) process that combines bipolar, CMOS and DMOS components. DMOS output transistors (MOSFETs) are used because of the absence of secondary breakdown, which gives a better SOAR performance. The internal circuits are designed in such way that only a few external components are needed to get a correct working application.

The TDA8358J is functional the same as the TDA8359J vertical deflection output stage. The TDA8358J differs in only one aspect from the TDA8359J; it has an additional East - West amplifier.

The TDA8358J is the successor for the TDA8350Q vertical deflection output stage with an east - west amplifier. There were two reasons to develop a successor. Reason number one was to have a better temperature distribution. This is done in a DMOS process in stead of Bipolar. Reason number two was to increase the output capacity of the East - West amplifier. The maximum East - West output voltage and maximum output current is increased.

1.1 Features.

- Few external components required
- High efficiency fully DC coupled vertical bridge output circuit
- Short rise and fall time of the vertical flyback switch
- Temperature (thermal) protection circuit
- Blanking pulse generator (guard)
- Improved EMC performance due to differential inputs
- East - West output stage

1.2 Ordering information.

Type Number	Package		
	Name	Description	Version
TDA8358J	DBS13P	plastic DIL-bent-SIL power package; 13 leads	SOT141

1.3 Block diagram

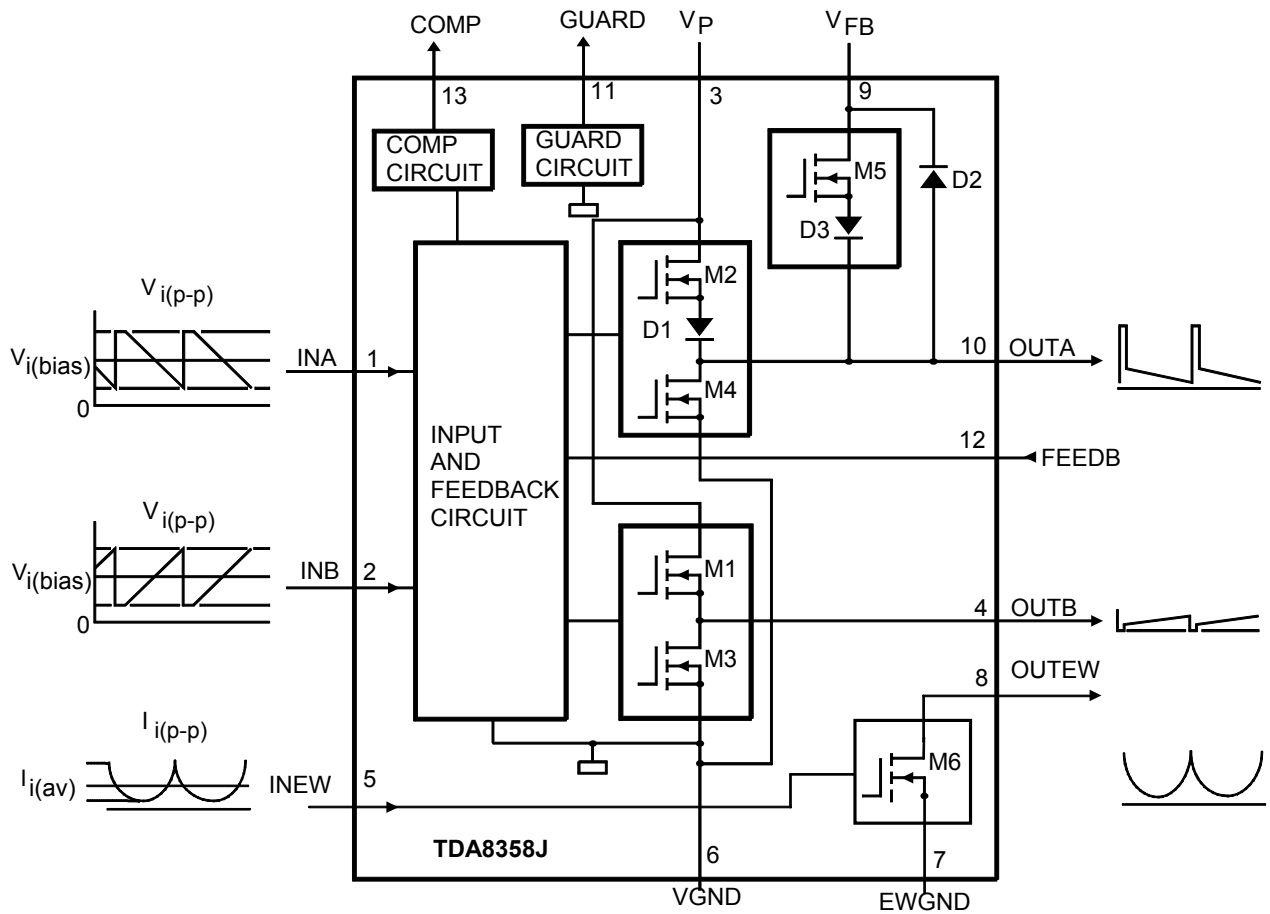
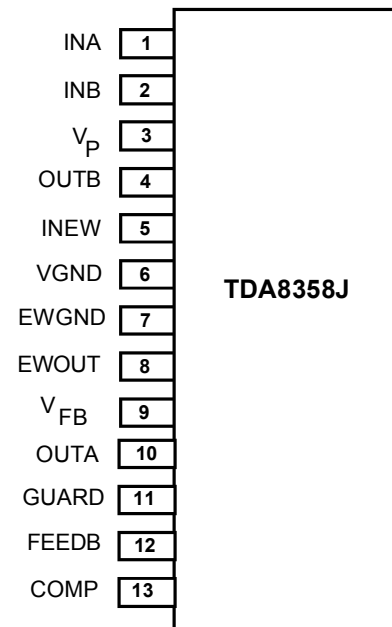


fig 1: Block diagram.

1.4 Pinning

Symbol	Pin	Description
INA	1	vertical input (positive)
INB	2	vertical input (negative)
V _P	3	supply voltage
OUTB	4	vertical output voltage B
INEW	5	East - West input voltage
VGND	6	Vertical ground
EWGND	7	East - West ground
OUTEW	8	East - West output voltage
V _{FB}	9	flyback supply voltage
OUTA	10	vertical output voltage A
GUARD	11	guard output voltage
FEEDB	12	input measuring resistor
COMP	13	input compensation current



1.5 Quick reference data

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies						
V _P	supply voltage		7.5	12	18	V
V _{FB}	flyback supply voltage		2xV _P	45	66	V
I _{q(P)(av)}	average quiescent supply current	during scan	-	10	15	mA
I _{q(FB)(av)}	average quiescent flyback supply current	during scan	-	-	10	mA
P _{tot}	total power dissipation		-	-	15	W
Input and output						
V _{i(dif)(p-p)}	differential input voltage (peak-to-peak value)		-	1000	1500	mV
I _{o(p-p)}	output current (peak-to-peak value)		-	-	3.2	A
Flyback switch						
I _{o(peak)}	maximum (peak) output current	t ≤ 1.5 ms	-	-	±1.8	A
East - West amplifier						
V _o	output voltage		-	-	68	V
V _{I(bias)}	input bias voltage		2	-	3.2	V
I _o	output current		-	-	750	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Thermal data; in accordance with IEC 747-1						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	ambient temperature		-25	-	+ 85	°C
T_j	junction temperature		-	-	+150	°C
$R_{th(j-c)}$	thermal resistance from junction to case		-	4	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	40	-	K/W

2. DEVICE DESCRIPTION AND APPLICATION INFORMATION

2.1 Internal pin configuration

Pin	Symbol	Equivalent circuit
1	INA	
2	INB	
3	V _P	
4	OUTB	
6	VGND	
9	V _{FB}	
10	OUTA	
5	INEW	
7	EWGND	
8	OUTEW	

MGL858

Pin	Symbol	Equivalent circuit
11	GUARD	
12	FEEDB	
13	COMP	

fig 2: Internal circuit configuration

2.2 Application diagram

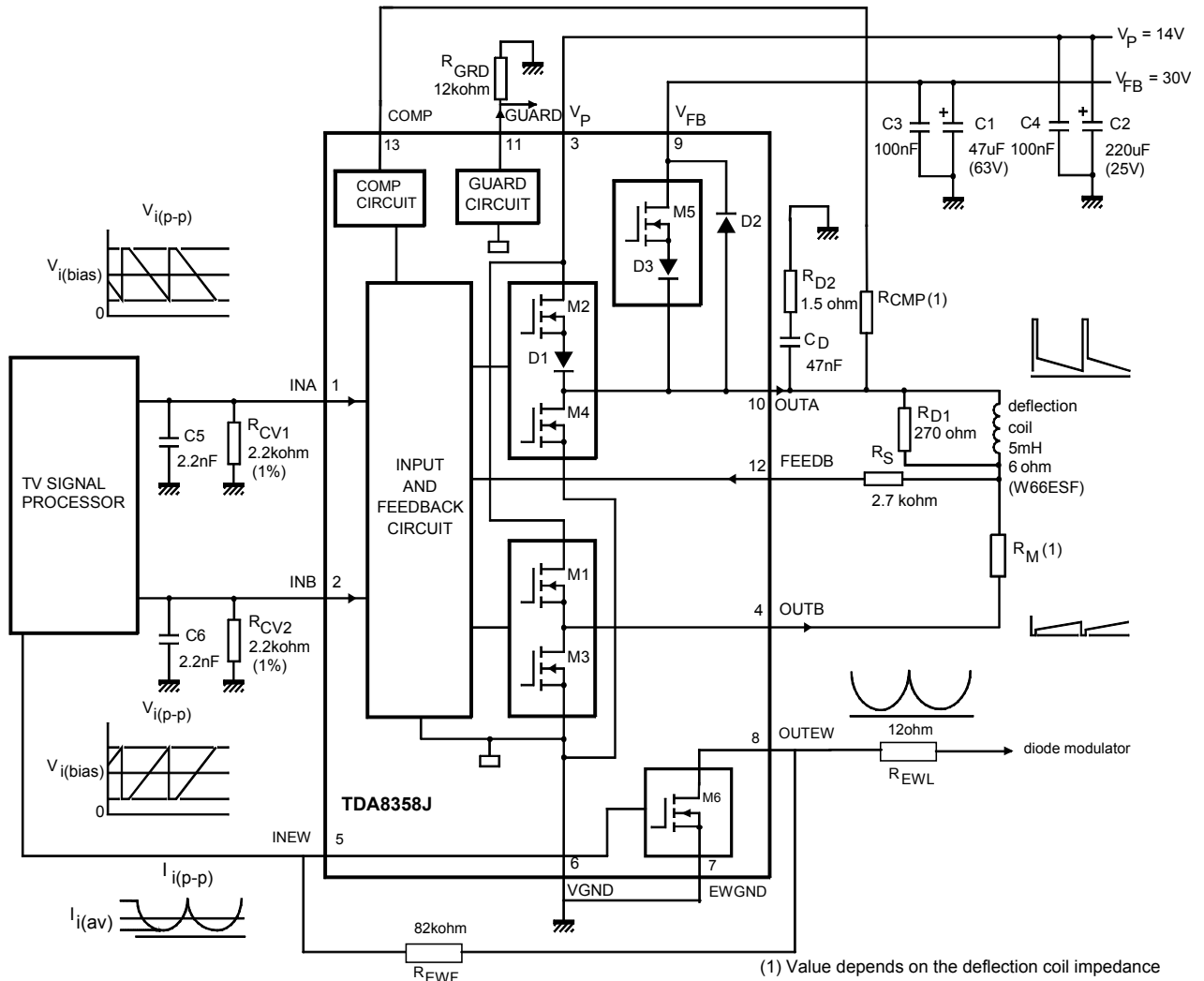


fig 3: Application diagram.

The TDA8358J is a vertical drive circuit in a bridge configuration. The output amplifiers are driven in opposite phase.

When looking at the application diagram, the following components can be described in short terms (detailed information is given in the succeeding sections).

The input circuit of the TDA8358J is a differential voltage driven input. The external resistors R_{CV1} and R_{CV2} convert the output currents of the TV signal processor into input voltages. The differential input voltage is compared with the voltage across the measuring resistor R_M that provides feedback information. The deflection coil is connected between OUTA and resistor R_M and OUTB.

The damping resistor R_{D1} is connected across the deflection coil for HF loop stability. The damping resistor compensation, which consists of a resistor R_{CMP} , compensates current differences in the damping resistor during scan and flyback and assures a short settling time.

2.3 Vertical amplifier

In many conventional deflection output circuits, the deflection coil must be AC coupled. This will require an expensive coupling capacitor of approximately 2200 μF . Beside higher costs, the coupling capacitor can cause picture bounce after switching between channels on the TV set. This capacitor can be omitted in a DC coupled deflection output circuit.

The TDA8358J is a DC coupled deflection output circuit, which has no bounce effect during channel switching. Also DC-coupling enables easy DC-shifting of the picture. By using differential mode inputs the EMC immunity is improved. The deflection coil and the measuring resistor R_M are connected between the output amplifiers of the TDA8358J that is driven in opposite phase. See fig 3.

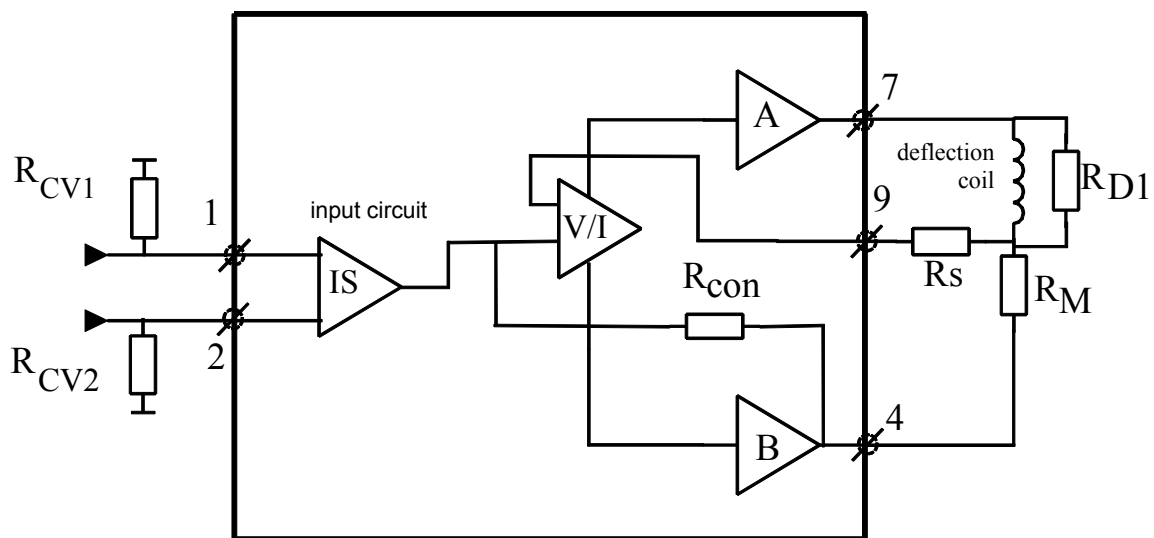


fig 4: Simplified block diagram of the vertical circuit.

Since the Input Stage (IS) is voltage driven, resistor R_{CV1} and R_{CV2} are used to convert the differential output current delivered by the TV signal processor (See fig 4). But TV signal processor circuits, which deliver an output voltage can also be used, in that case resistor R_{CV1} and R_{CV2} are not necessary.

The voltage across the internal conversion resistor R_{con} is compared with the output current through the deflection coil, measured as a voltage across the measuring resistor R_M , by means of a voltage current converter V/I . The output amplifiers A and B will be driven until both voltages are equal. This means that the deflection current is determined by the ratio of the input resistors $R_{CV1,2}$ and the measuring resistor R_M .

The output current is adjustable up to 3.2 A_{p-p} mainly by varying resistor R_M . The peak to peak input voltage should be as high as possible (maximum 1.5V) for having an optimal reducing of distortion on the input signals. The maximum input voltage (bias + peak voltage) is 1.6V. The minimum input voltage (bias - peak voltage) is 100 mV, however for an optimum linearity a minimum input voltage of 300 mV is recommended.

2.4 Vertical input circuit

Pin 1 INA and pin 2 INB

The input circuit is a differential voltage driven input. The input circuit is specially designed for direct connection to TV signal processors delivering a differential signal, but it is also suitable for single-ended applications See 2.4.2. For processors with output currents, the currents have to be converted to voltages by the conversion resistors R_{CV1} and R_{CV2} connected to pins 1 INA and 2 INB. Some type numbers of suitable drive circuits: TDA9151B, TDA9160A, TDA9162, TDA933X, TDA8366, TDA8367, TDA837X, TDA884X/5X (one chip family), TDA886X/7X/8X (bocma family), TDA935X/6X/8X and TDA955X/6X/8X (ultimate one chip family) and TDA485X (deflection processor family).

An example of the vertical drive output signal of an “ultimate one chip” family IC is given below. The drive signal depends on which drive circuit is used. In the ultimate one chip family, the zoom is standard enabled and is set to a value of 25 (dec) on a range of 0 – 63. This causes a small flat piece just before the start of the scan.

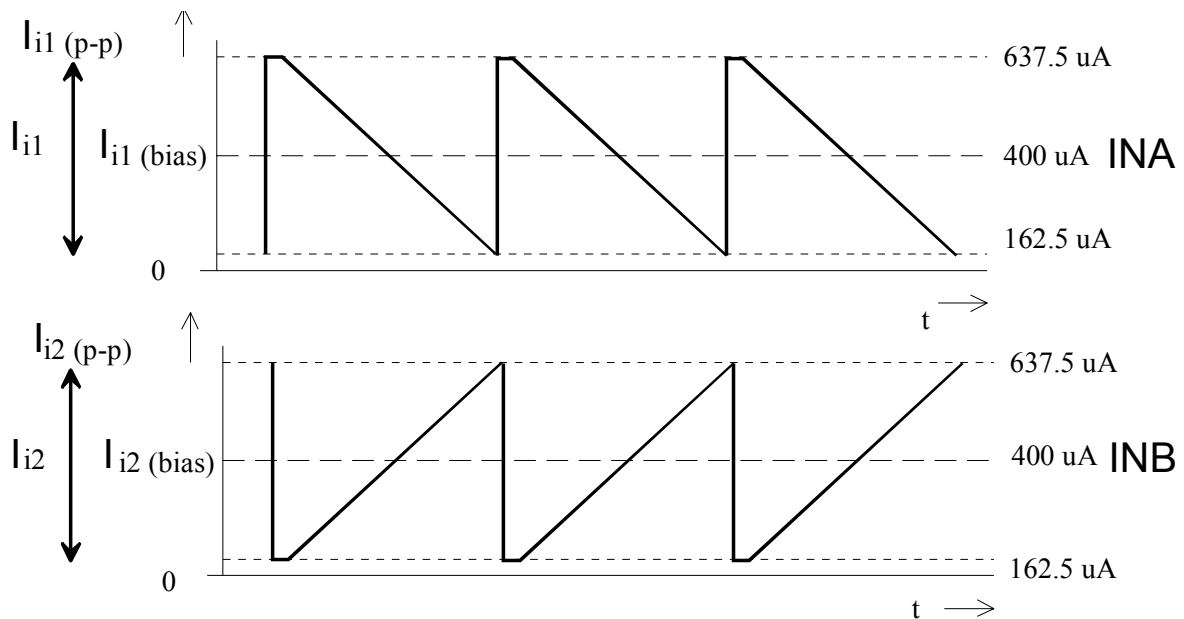


fig 5: Vertical drive output currents of the TDA935X/6X/8X / TDA955X/6X/8X family.

The bias output signal current is 400 μA typical. The differential mode peak to peak output current is typical 475 μA_{P-P} .

After connecting the TDA935X/6X/8X / TDA955X/6X/8X family to the TDA8358J, the following waveforms appear on the input pin 1 INA and pin 2 INB when the conversion resistors R_{CV1} and R_{CV2} are 2k2.

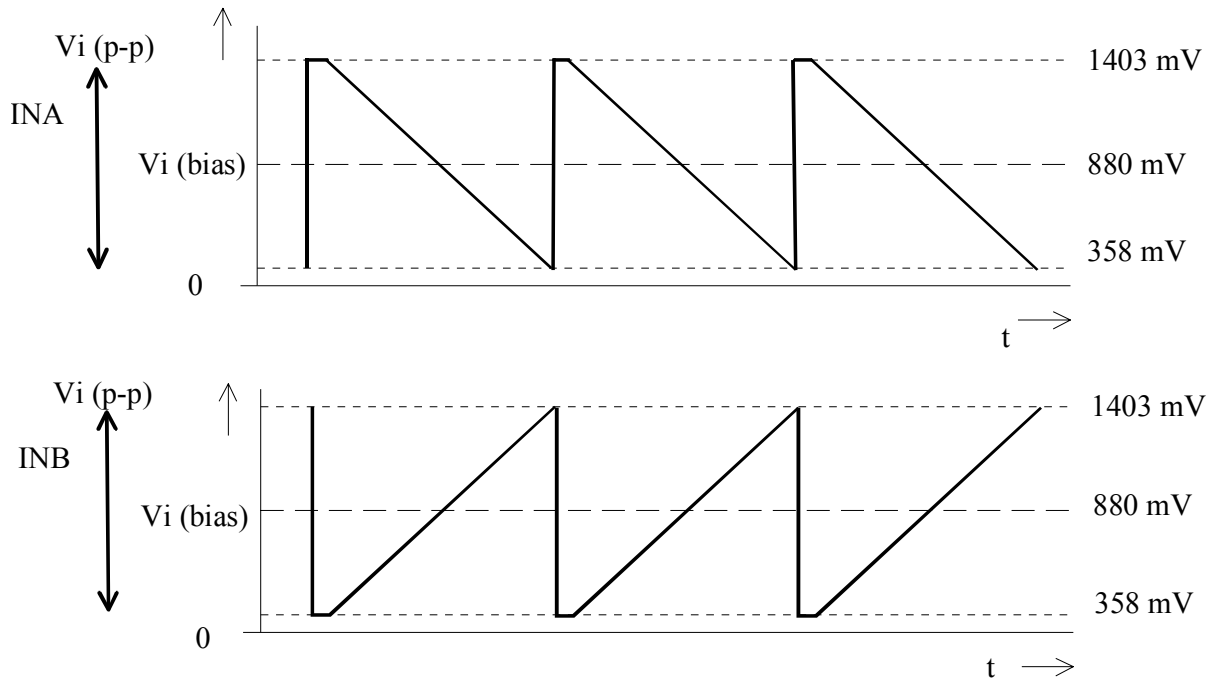


fig 6: Input voltages on pin 1 INA and pin 2 INB of TDA8358J.

The differential voltage on the input ($V_{INA} - V_{INB}$) is as follows:

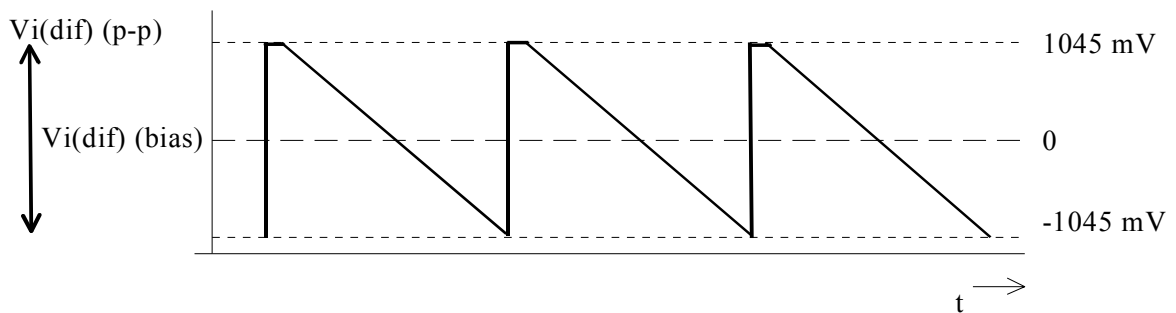


fig 7: Differential input voltage ($V_{INA} - V_{INB}$)

The internal input configuration is symmetrical to have a good EMI behaviour, so the external input configuration should also be symmetrical. This means that the drive tracks should be as short as possible and routed next to each other.

The input configuration is as follows:

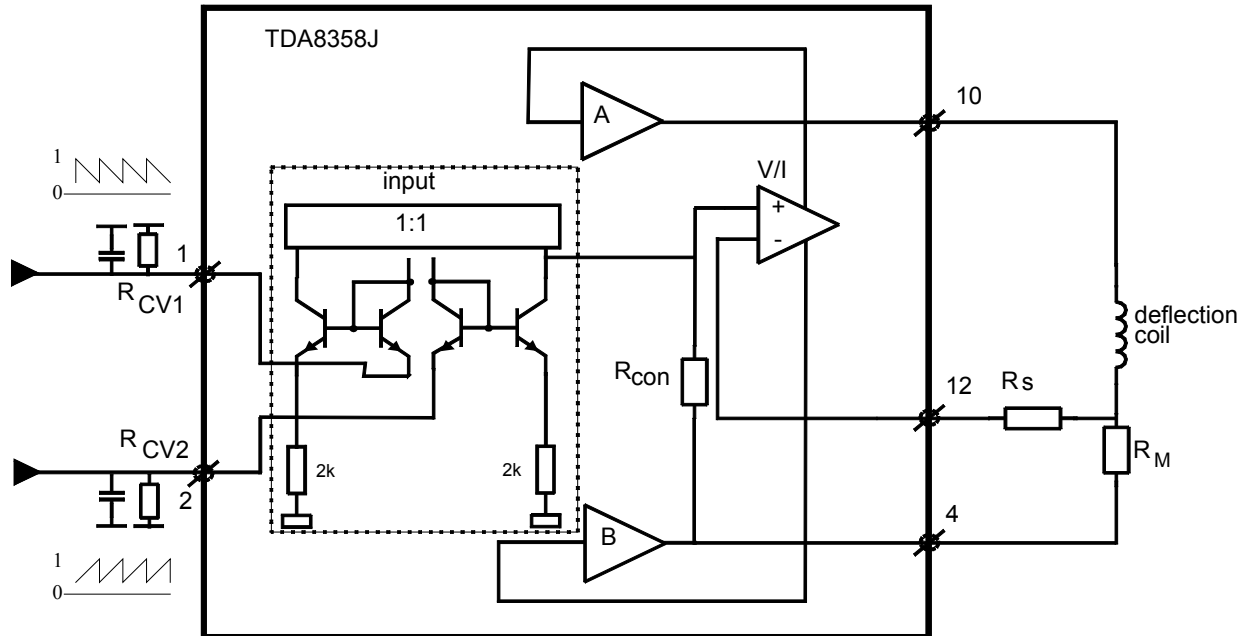


fig 8: Input configuration.

The differential input voltage is compared with the voltage across the measuring resistor R_M , providing the feedback information. The voltage across R_M is proportional to the output current. The relationship between the differential input voltage and the output current is defined by:

$$V_{i(dif)(p-p)} = I_{o(p-p)} \times R_M$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB} \quad (\text{See fig 7.})$$

V_{INA} = voltage INA

V_{INB} = voltage INB

$I_{o(p-p)}$ = output current through the deflection coil and R_M , peak to peak value

R_M = measuring resistor

The next figure gives the vertical drive circuit diagram of the TDA935X/6X/8X / TDA955X/6X/8X family with the vertical output stage TDA8358J.

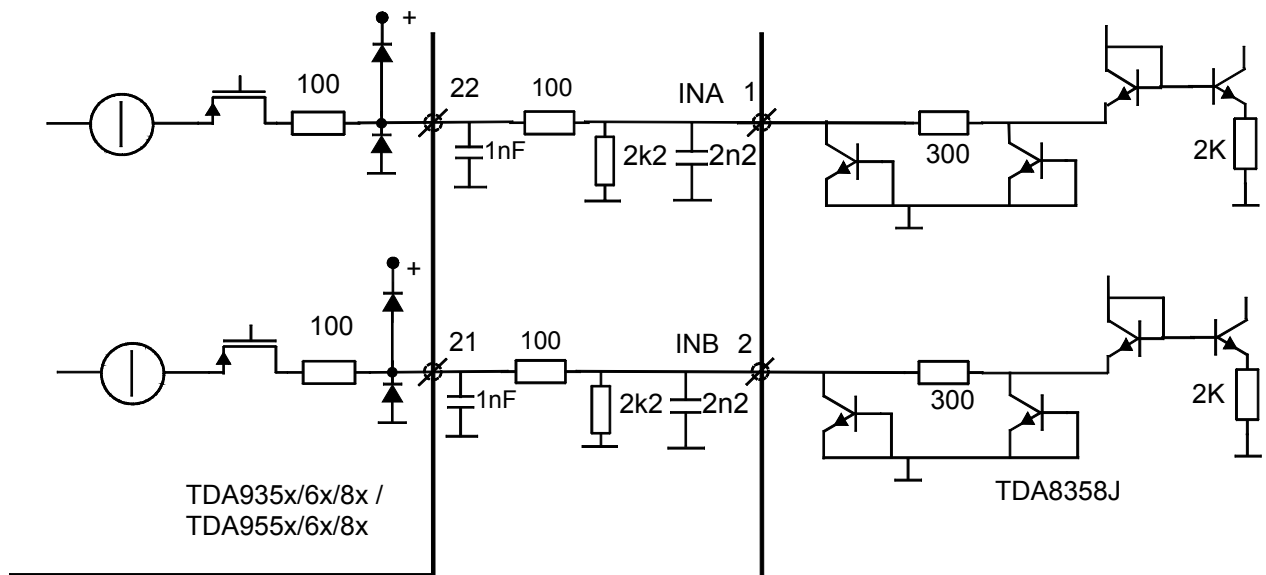


fig 9: Interconnect between TDA935x/6x/8x / TDA955x/6x/8x and TDA8358J

2.4.1 Conversion resistors $R_{CV1,2}$ and measuring resistor R_M

Most of the TV signal processors of Philips have a current output. This current has to be converted by resistors R_{CV1} and R_{CV2} at the input of the TDA8358J.

The peak to peak input voltage $V_{i(p-p)}$ should be as high as possible (maximum 1.5V) for an optimal reducing of the differential distortion on the input signals. So R_{CV1} and R_{CV2} have to be chosen so that $V_{i(p-p)}$ is as high as possible. See fig 6. The maximum input voltage (bias + peak voltage) on pin 1 INA and pin 2 INB is 1.6V. The minimum input voltage (bias - peak voltage) is 100 mV, however a minimum input voltage of 300 mV is recommended because of an optimum linearity.

The conversion resistors R_{CV1} and R_{CV2} must have the same value and can be calculated by: (See fig 5 and fig 6)

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i,2(bias)} + \frac{I_{i,2(p-p)}}{2}} \quad \text{or} \quad R_{CV1,2} = \frac{V_{i(bias)} - V_{i(peak)}}{I_{i,2(bias)} - \frac{I_{i,2(p-p)}}{2}}$$

$V_{i(bias)} + V_{i(peak)}$ = should be < 1.5V for room for vertical alignment. (Maximum input voltage = 1.6V)

$V_{i(bias)} - V_{i(peak)}$ = should be > 0.3V for optimum linearity

$I_{i,2(p-p)}$ = peak to peak output current given from the TV signal processor.

$I_{i,2(bias)}$ = bias output current given from the TV signal processor

For the TDA935X/6X/8X or TDA955X/6X/8X family the value of R_{CV} is:

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i(bias)} + I_{i(peak)}} = \frac{1.5}{400 + \frac{475}{2}} = 2350\Omega$$

So $R_{CV1,2}$ must be 2k2

The output current is adjustable up to 3.2 A_{p-p} for the TDA8358J by varying R_M .

The measuring resistor R_M can be calculated by means of the formula:

$$R_M = \frac{V_{i(dif)(p-p)}}{I_{o(p-p)}}$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB}$$

$$V_{i(dif)(p-p)} = I_{i1(p-p)} * R_{CV1} - (-I_{i2(p-p)} * R_{CV2})$$

Example for TDA8358J with the TDA935X/6X/8X or TDA955X/6X/8X family as TV signal processor:

We suppose the following:

$$\begin{aligned} I_{O(p-p)} &= 2.4 \text{ A}_{pp} \\ I_{i(p-p)} &= 475\mu\text{A} \text{ (value is given by TV signal processor)} \\ V_{i(p-p)} &= 1045 \text{ mV (see fig 6)} \end{aligned}$$

$$R_M = \frac{2.09V}{2.4A} = 0.87\Omega$$

2.4.2 Example of a single driven application with TDA8358J

It is also possible to drive the TDA8358J with a single drive signal, however differential driven is recommended. The single drive signal must be connected to pin 1 INA. Pin 2 INB needs then a stable DC voltage with a value of about the same as the bias voltage on pin 1 INA. A capacitor with a value of 10nF must be connected between pin 1 INA and pin 2 INB for stability. See fig 10. The measuring resistor R_M must be half the value of when the TDA8358J is differential driven. The value of the compensation resistor must be twice the value of when the TDA8358J is differential driven.

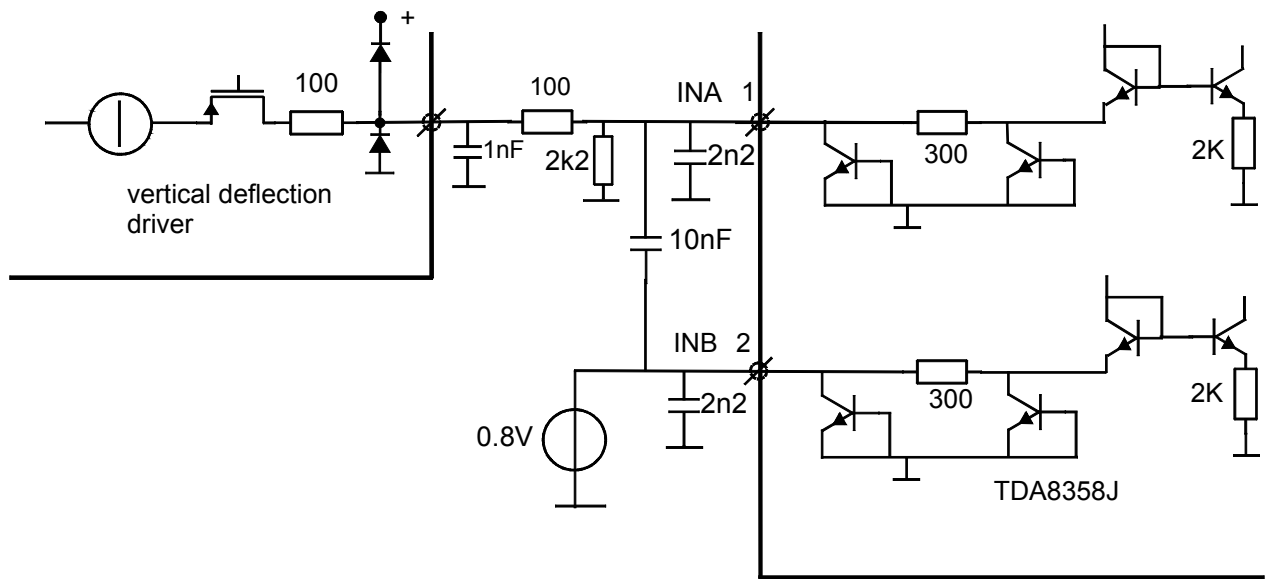


fig 10: Example of a single driven application

2.5 Feedback Circuit

Pin 12 FEEDB

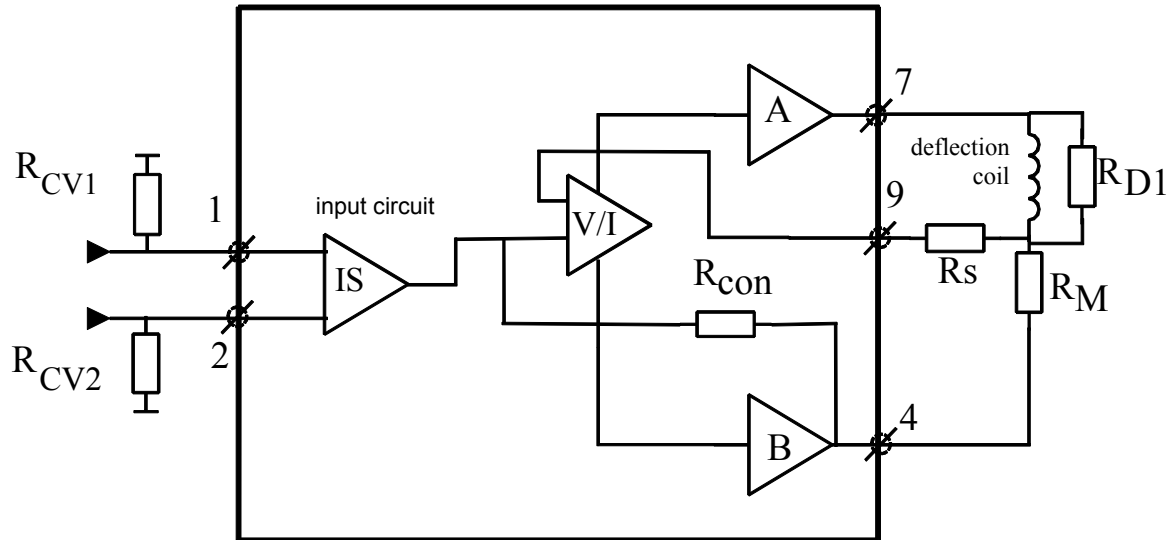


fig 11: Feedback circuit.

The feedback circuit is built up with a reference between pin 4 (OUTB) and pin 12 (FEEDB), the voltage across R_M and a series resistor R_S (pin 12). The input circuit is connected to a differential V/I converter, which compares the voltage across R_M and the voltage across the internal conversion resistor R_{CON} . If both voltages are not equal the V/I converter drives the output stages until the voltage across R_M is equal to the voltage across R_{CON} .

2.5.1 Series resistor (R_S)

The purpose of the series resistor R_S at pin 12 FEEDB is to achieve equal impedance for the V/I converter, $R_S = R_{CON}$ because the V/I converter, see fig 11, should see equal input impedance at both inputs. This improves the common mode suppression. The tracks to the inputs are not the same. One track is connected internally to resistor R_{CON} . The other input has an external wire. To match R_{CON} , the series resistor R_S is connected between the deflection coil and pin 12. Choose the value of R_S about $2.7k\Omega$.

If the output waveform should contain some oscillations, the value of R_S can be slightly changed. A small capacitor of 1pF-100pF between pin 12 (FEEDB) and pin 4 (OUTB) could also help to suppress minor oscillations.

2.6 Vertical output stage

Pin 4 OUTB and pin 10 OUTA

The Philips TDA8358J vertical output stage uses a class G bridge concept. (see fig 12). In the class G concept the flyback supply voltage can be chosen independent from the main supply voltage. This allows a very efficient DC coupling of the vertical output stages. This matches perfectly with modern driving circuits, which can change settings like amplitude, shift, slope and s-correction, which are controlled via the I²C bus. The vertical deflection coil in series with resistor R_M is connected between the two outputs pin 10 OUTA and pin 4 OUTB. Resistor R_M is used to measure the current through the coil. The voltage across resistor R_M is the input voltage for the feedback stage.

The two output amplifier stages A and B are nearly identical. Output stage top MOSFET A (M2), diode D1 and bottom MOSFET B (M3), conduct for the first part of the sawtooth (coil) current and are supplied from the main supply (V_P). Output stage top MOSFET B (M1) and bottom MOSFET A (M4) conduct for the second part of the sawtooth current and are also supplied via the same main supply voltage.

MOSFET (M5) is the flyback switch. It is supplied through a higher supply voltage (V_{FB}) than the main supply voltage to achieve a short flyback time.

The maximum allowed values of the main supply voltage is 18 Volt and for the flyback supply voltage 66 Volt.

To prevent a short circuit between the main supply and the flyback supply, a diode (D1) is placed in series with the top MOSFET A (M2) of the output stage. To prevent conduction of the parasitic diode of the flyback switch (M5), (during the first part of the flyback period) a diode (D3) is placed in series with it.

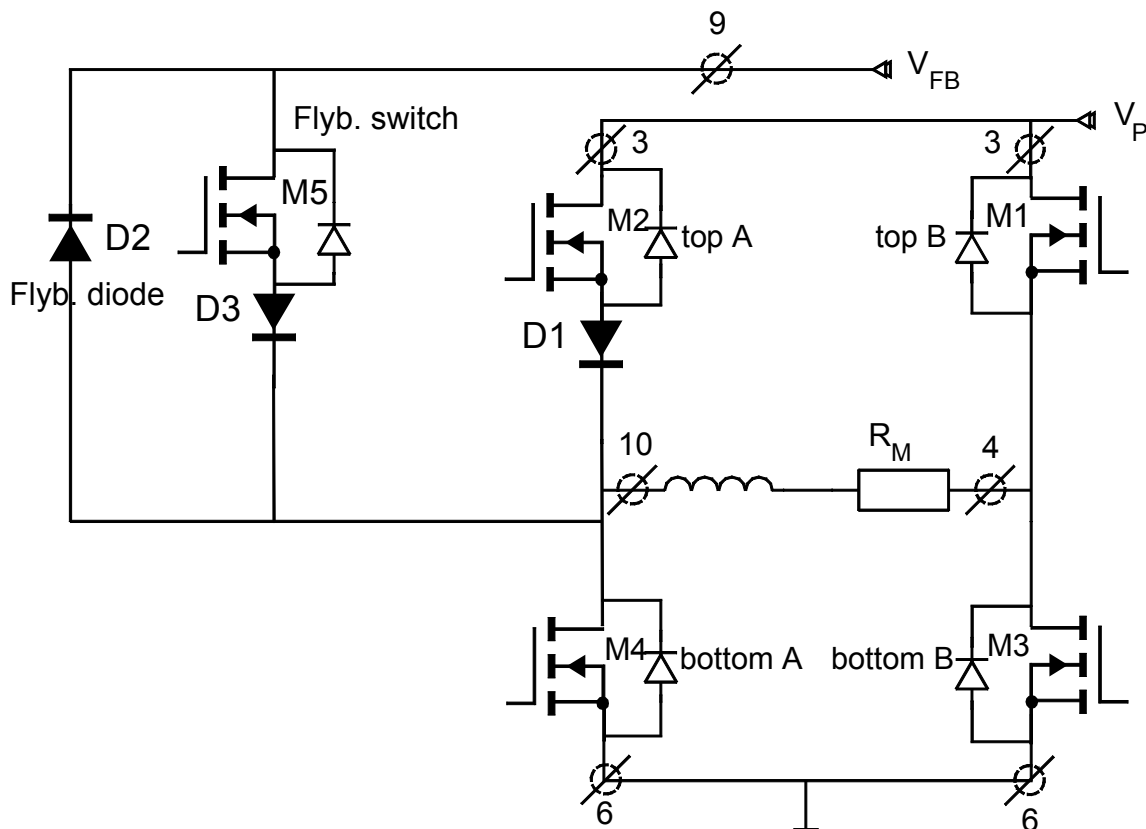


fig 12: Output configuration TDA8358J.

The current flow through the output MOSFETs and the vertical deflection coil can be considered in four different parts/stages: the first part of the vertical scan, the second part of the vertical scan, the first part of the flyback and the second part of the flyback. The first and second part of the vertical scan will be discussed in this section, while the flyback part will be explained in the next section (2.7)

The current path in the vertical output bridge for the first part of the scan is illustrated by the dotted line in fig 13.

In this figure one can see that the current flows from the main supply pin via top MOSFET A (M2) and diode (D1) of output A in the vertical deflection coil and measuring resistor R_M , via bottom MOSFET B (M3) of output B to ground.

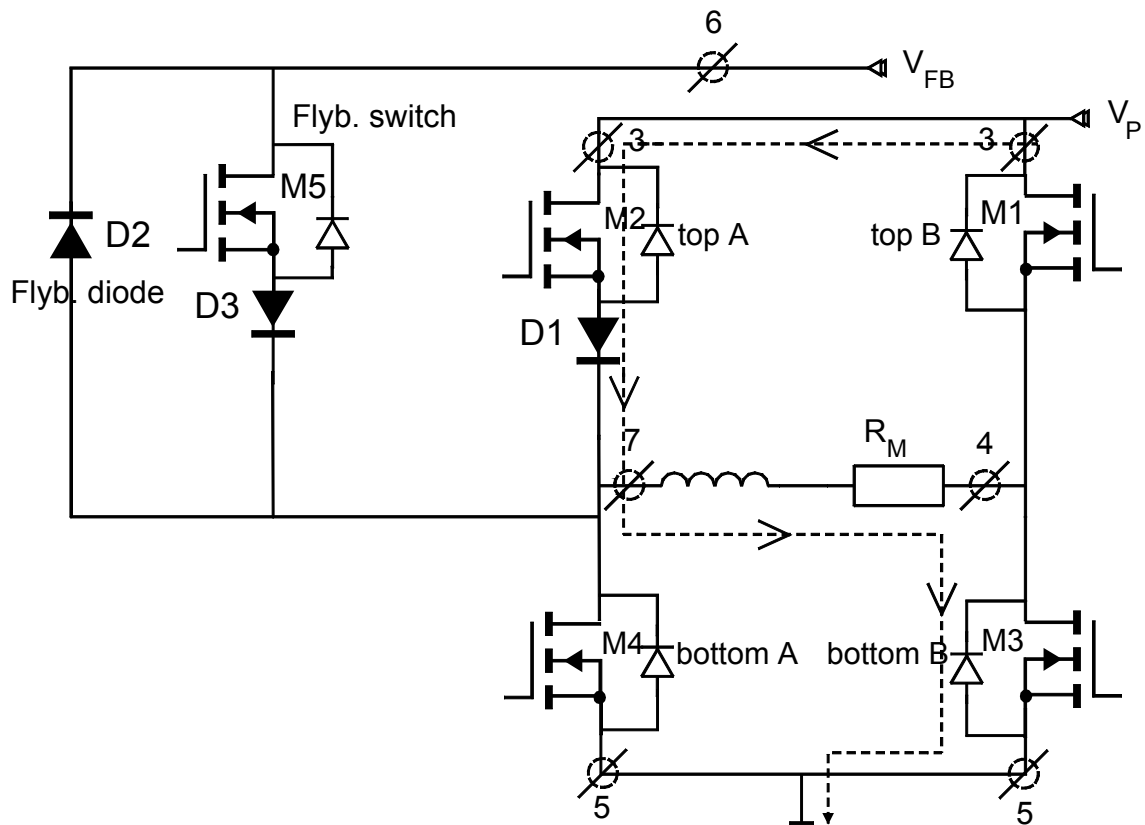


fig 13: Current path in first part of scan.

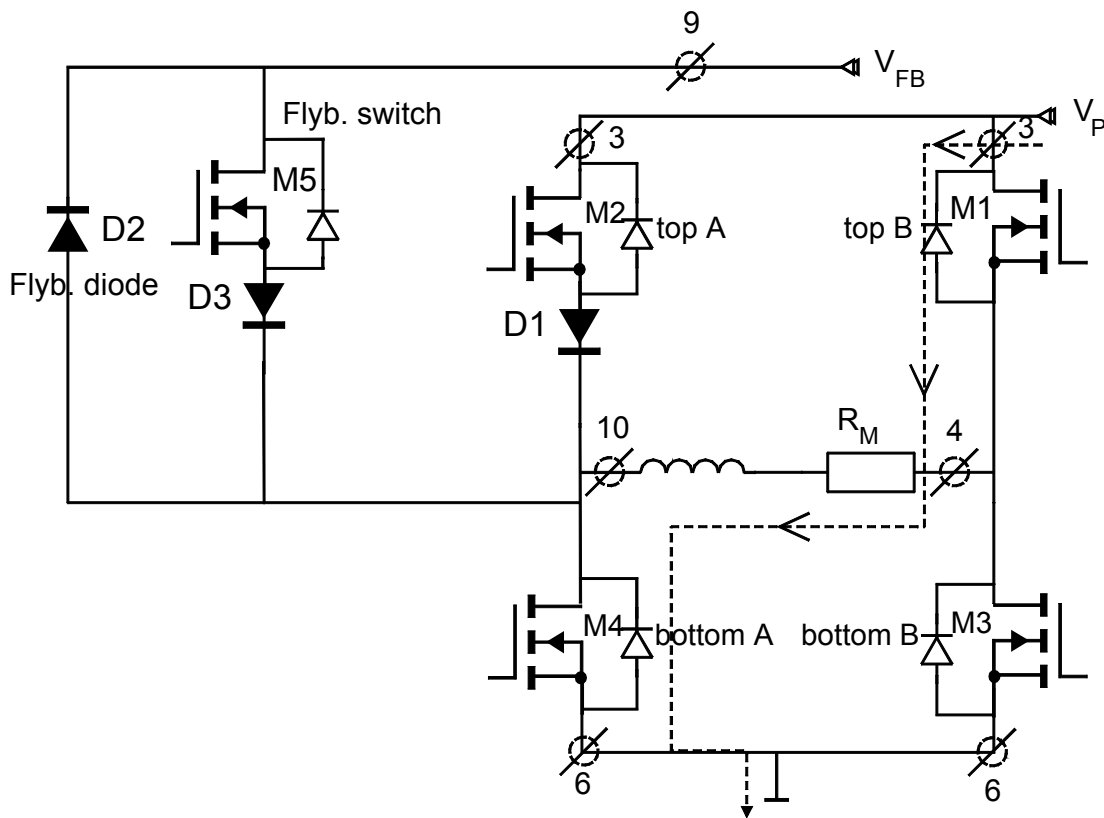


fig 14: Current path in second part of scan.

The current path for the second part of the scan is illustrated by the dotted line in fig 14. During the second part of the scan time, the current flows from the main supply pin via top MOSFET B (M1) via output B in the measuring resistor R_M and the vertical deflection coil, via bottom MOSFET A (M4) of output A to ground. During the scan time, the current that flows through the deflection coil has a sawtooth shape and the main supply (V_P) supplies the current that is needed.

The supply current will be at its maximum at the start of the scan, decreasing to the middle of the scan and then increasing until the end of the scan.

In fig 15 and fig 16 waveforms during scan are shown, these pictures are made with a digital oscilloscope. In fig 16 it is seen that the lines of output voltages A and B contain a small jump, when switching from the first part of the scan to the second part of the scan. This is because diode D1 causes a voltage drop. This is not crossover. The line of the output current is linear.

Furthermore one can see that the lines of the Output A voltage and the Output B voltage do not cross in the middle of the scan time. This is because the voltage drop across the deflection coil, for the first part of the scan is different than the voltage drop across the deflection coil during the second part of the scan. This is caused by the coil impedance, which exists of a resistive part and an inductive part. So the total voltage drop across the deflection coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign. See also section 2.11.1.

So, if the deflection coil has a *relatively large* L (inductance), the voltage drop during the *first part* of the scan has a *lower value* compared to the value of the second part of the scan. That's why the crossing point of the lines of output A and output B shifts to the left, when the L of the vertical deflection coil increases.

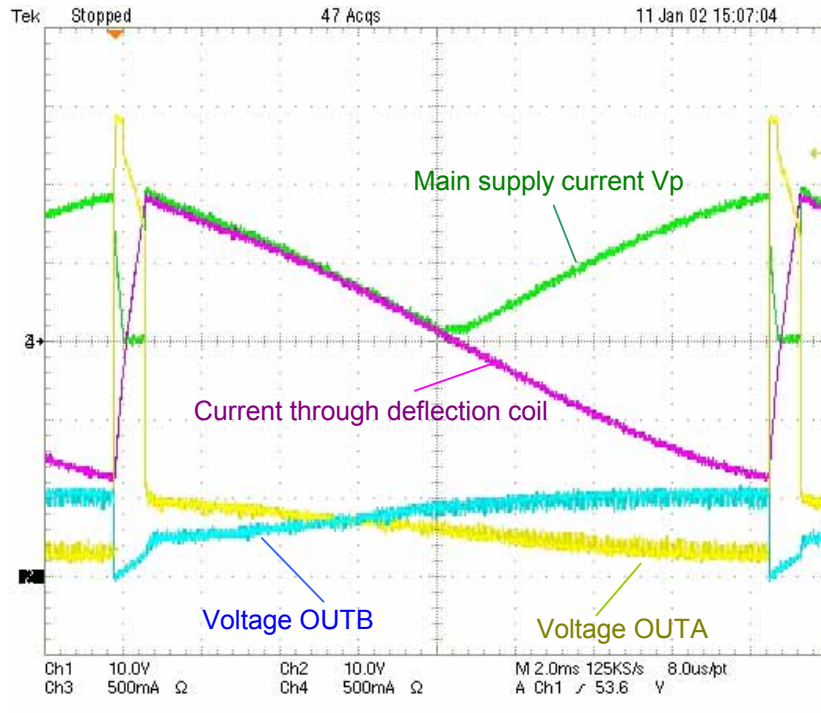


fig 15: Waveforms during scan.

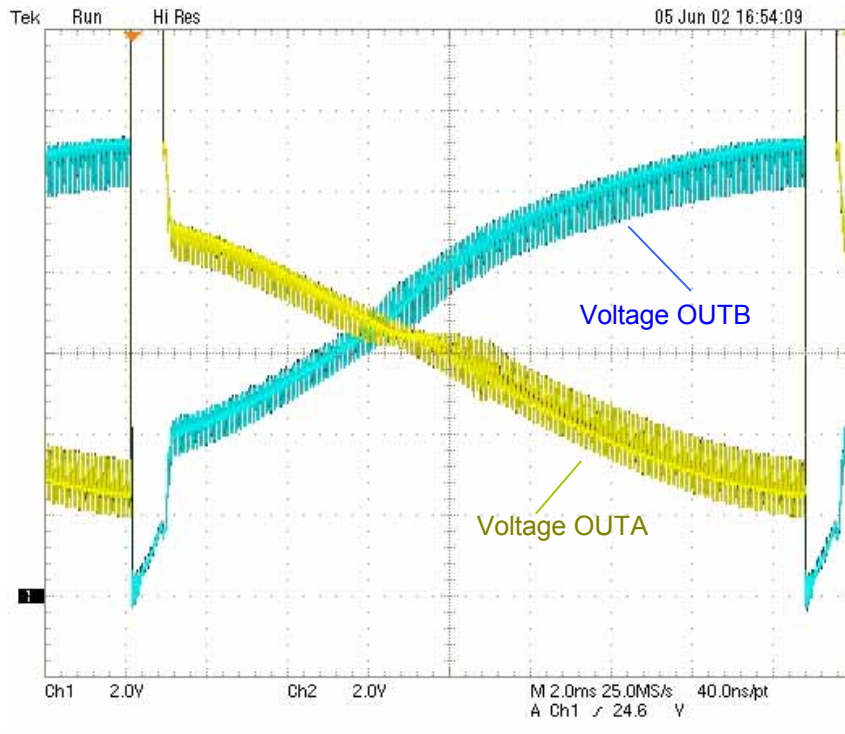


fig 16: Jump in output voltage

2.7 The flyback switch

Pin 9 V_{FB} and pin 10 OUTA

In the TDA8358J concept the value of the supply voltage (V_P) and the flyback supply voltage (V_{FB}) can be chosen independently (class G). In general, the flyback supply voltage will be chosen much higher than the supply voltage that is needed for the scan. A ratio of 2 to 4 is possible, with a maximum of 66 Volt. This is much higher than the value that is reached in conventional designs with a flyback voltage generator circuit (in general a ratio of 2, maximum). The flyback supply voltage is almost fully available at the output pin of stage A, thus across the deflection coil.

At the end of the scan time the input drive voltage will change fast in direction. The coil will try to maintain the present current level. At this moment the output signal cannot follow the input signal, which forces the amplifier into an open-loop condition. The flyback pulse will start.

The flyback can be divided in part A and B, see fig 17. Due to the high voltage across the coil and the influence of the damping resistor, the first part A has a short duration. Part A ends when the current in the deflection coil becomes zero.

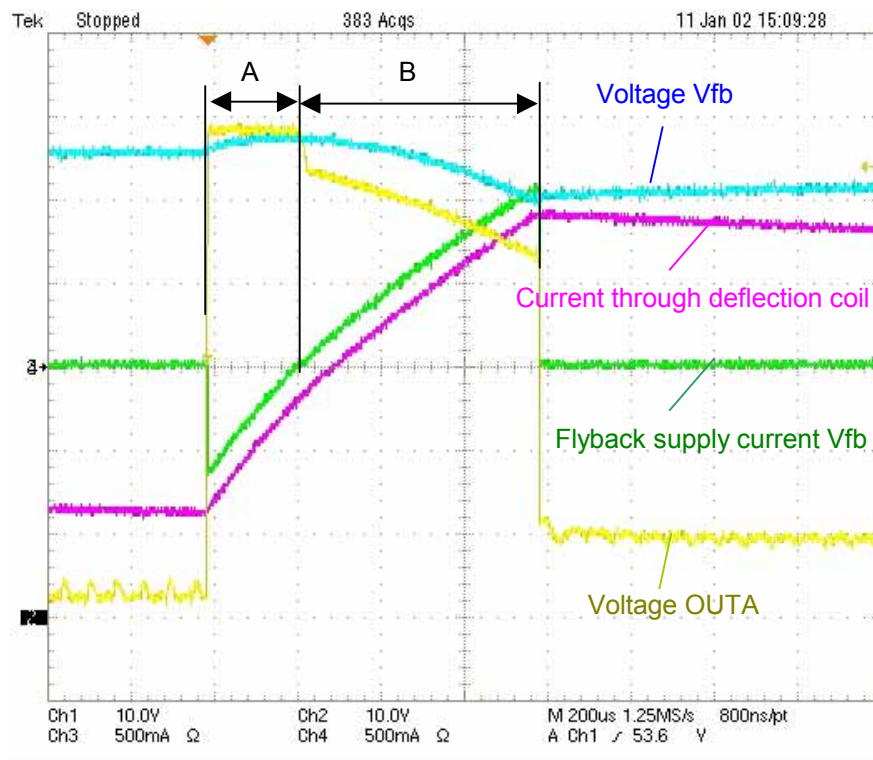


fig 17: Waveforms during flyback.

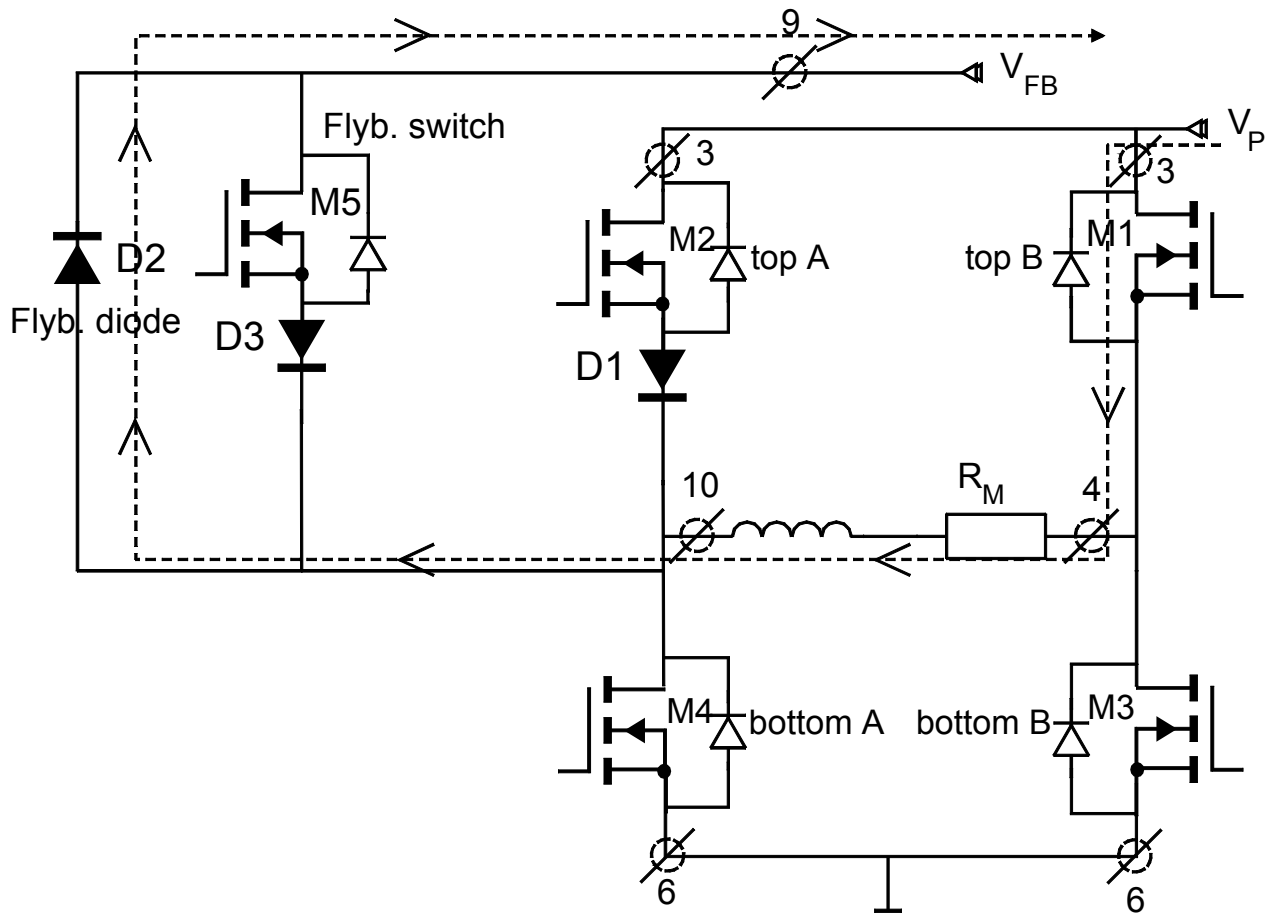


fig 18: Current path in first part of flyback.

At the start of the first part of the vertical flyback the internal drive signal switches off the top MOSFET of stage B (M1).

The current in the deflection coil seeks a way out and the voltage at the output pin 10 OUTA increases and so the voltage at pin 4 OUTB will drop and tries to go below zero. Now, a clamp is activated to keep this voltage above zero. This clamp will switch-on again MOSFET M1, otherwise the parasitic diode across bottom MOSFET M3 would conduct which could cause substrate-currents which could cause a malfunction of the device.

The voltage at the output (pin 10) increases and the flyback diode D2 conducts. This output voltage becomes about 2 Volt higher than the flyback supply voltage (=voltage across diode D2), see fig 17. The current is fed into the flyback supply capacitor.

The current goes now through the top MOSFET of stage B (M1), the external measuring resistor R_M , the deflection coil and the internal flyback diode (D2) into the flyback supply, see the dotted line in fig 18.

The current flow for the second part "B" of the vertical flyback is given below.

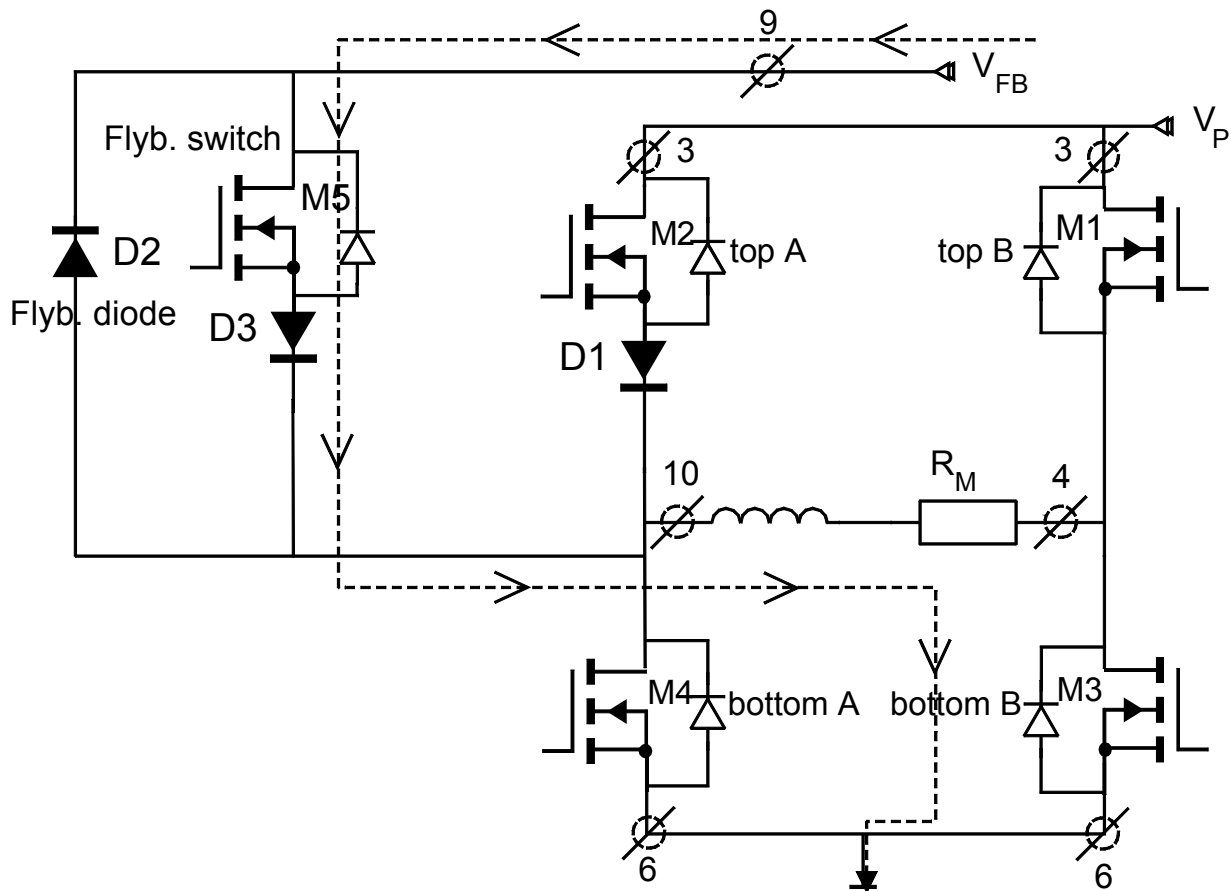


fig 19: Current path in second part of flyback.

The second part, part B of the flyback pulse, starts when the current in the deflection coil crosses the zero level, see fig 17. Now, the current in the deflection coil is supplied by the flyback voltage supply and the flyback switch (M5) conducts. The current flows via the flyback switch (M5), the internal diode (D3), the deflection coil, the measuring resistor R_M , via the bottom MOSFET of stage B (M3) to ground, see fig 19. (Due to a voltage loss across the flyback switch (M5) + the internal diode (D3), the output voltage at pin 7 is about 8 V lower than the flyback supply voltage. This voltage drop depends on the current in the coil; a higher current means a higher loss and thus a higher voltage drop.

The current through the coil will become positive now and will increase until the voltage value measured across R_M equals the input voltage. Then the feedback loop is closed and the flyback switch is switched off. The scan sequence can start again.

2.7.1 Adaptive control of the flyback switch

The waveform during part B of the flyback waveform has a shape that is created by the adaptive control of the flyback switch, which operates as follows. The output current of the flyback switch is measured on a certain level onwards, the drive of the flyback switch is increased, thus lowering the impedance of the flyback switch at increasing flyback current.

In the TDA8358JN2 the adaptive control circuit is activated at all values of the output current. This results in a lower dissipation in the flyback switch and a somewhat shorter flyback time. In the TDA8358JN1 the adaptive control circuit is not activated at a low output current. The small difference in the output voltage is given in fig 20:

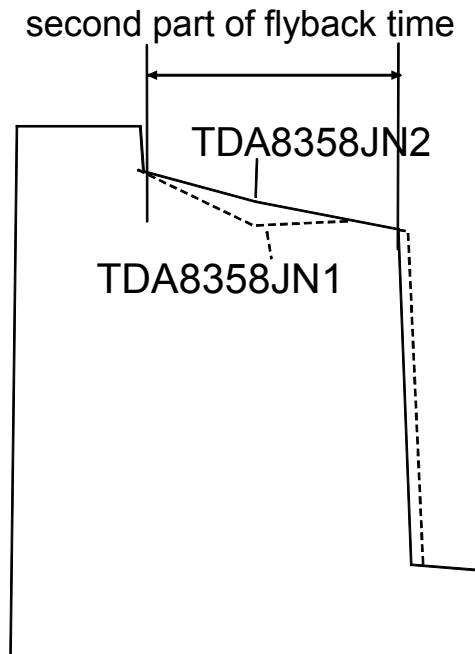


fig 20: Small difference in output voltage (flyback pulse) between N1 and N2

2.8 Damping resistor R_{D1} and damping resistor compensation circuit

Pin 13 COMP

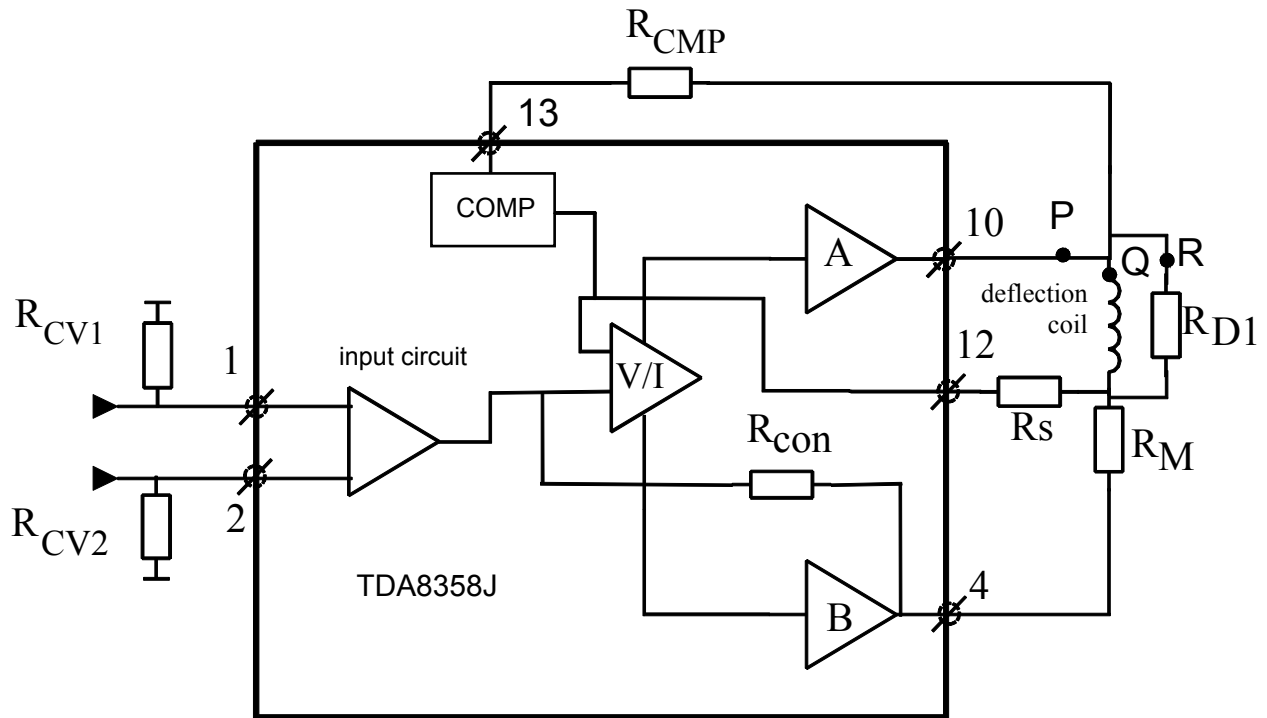


fig 21: Damping resistor compensation.

2.8.1 Damping resistor R_{D1}

A damping resistor is connected across the deflection coil to smooth the switch points of the current and voltage as well to prevent ringing. The value of R_{D1} depends on the deflection coil and it should be as high as possible. Choose the value of R_{D1} about 270Ω . **Be aware that there can be a damping resistor mounted on the deflection coil on the picture tube.**

If the damping resistor is situated on the deflection coil on the picture tube, the following picture fig 22, is seen *by measuring the current through the wires from the PCB to the deflection coil connector* (point P in fig 21). The damping resistor causes the difference in current values between points P and Q during flyback. During the flyback time period a higher current flows through the damping resistor than during scan time due to a higher voltage across the deflection coil.

If the value of the damping resistor is too high, the peak to peak voltage of line frequency ripple on the vertical output voltage will be too high. The impedance of the deflection coil is higher than the value of the damping resistor.

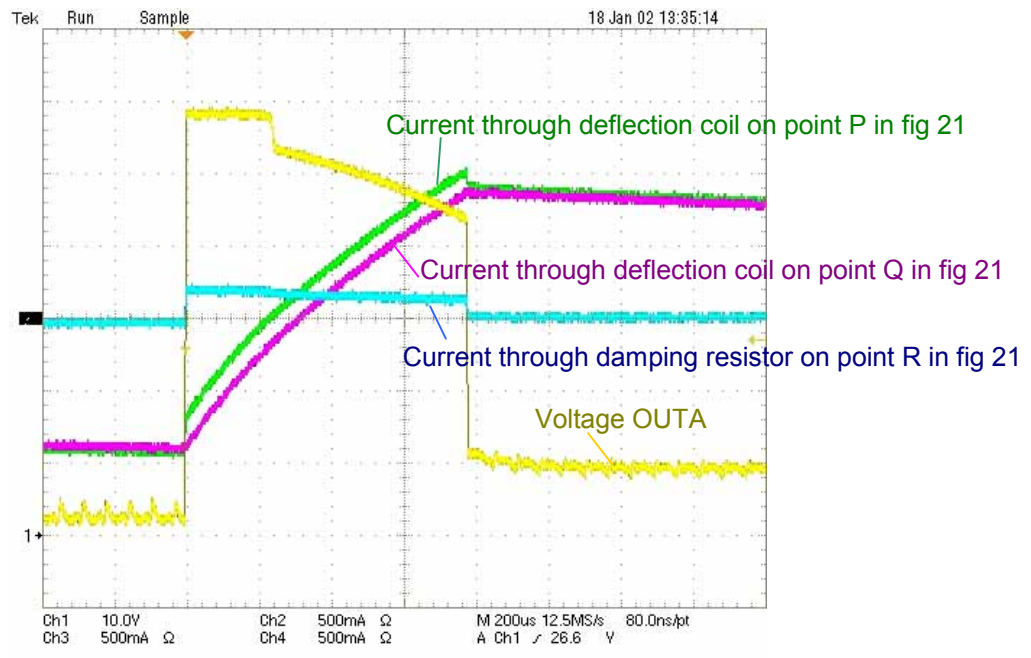


fig 22: Current through deflection coil measured on point P, Q and R in fig 21.

2.8.2 Damping resistor compensation circuit

The current values in the damping resistor R_{D1} during scan and flyback are significantly different. During the flyback time period a higher current flows through the damping resistor due to a higher voltage across the deflection coil. For example with $V_{FB} = 55V$ and $R_{D1} = 300\Omega$, the current through R_{D1} during flyback time is $55V/300\Omega = 183mA$. With a main supply voltage V_P of $14V$, the current through R_{D1} during scan time is $14V/300\Omega = 47mA$. Both the damping resistor current and the deflection coil current flow into the measuring resistor R_M . During flyback time the current in the measuring resistor R_M is higher than the intended current in the deflection coil. So a too low current flows into the deflection coil compared to the input signal during flyback time. This has an influence on the time the flyback switch is conducting. So without compensation the flyback switch stops conducting too soon and the flyback pulse width is too small. Now it will take a rather long time to reach the output current which equals the input signal. This results in a too low deflection coil current at the start of the scan.

The differences in the damping resistor current values during scan and flyback have to be compensated in order to achieve a short settling time. For that purpose a compensation resistor is connected between pin 10 OUTA and pin 13 COMP. See fig 21.

2.8.3 Calculation of the compensation resistor R_{CMP}

The value of the compensation resistor depends on:

- The flyback voltage supply; V_{FB}
- The internal voltage loss of the current path between pins V_{FB} and OUTA. So the voltage loss across the flyback switch M5 and diode D3; $V_{loss(FB)}$. See fig 19.
- The voltage of the main supply voltage; V_P .
- The value of the damping resistor; R_{D1}
- The value of the series resistors on pin 12 FEEDB; R_S
- The peak to peak output current; $I_{o(p-p)}$
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; R_M

The compensation resistor R_{CMP} is calculated in the following way:

$$R_{CMP} = \frac{(V_{FB} - V_{loss(FB)} - V_P) \times R_{D1} \times (R_S + 300)}{\left(V_{FB} - V_{loss(FB)} - \frac{I_{o(p-p)}}{2} \times R_{coil(hot)} \right) \times R_M}$$

Example of calculating R_{CMP} :

$$\begin{aligned} V_{FB} &= 30V \\ V_{loss(FB)} &= 8V \\ V_P &= 14V \\ R_{D1} &= 270\Omega \\ I_{o(p-p)} &= 2.4A \\ R_{coil(hot)} &= 6\Omega \times 1.2 = 7.2\Omega \\ R_M &= 0.87\Omega \\ R_S &= 2.7k\Omega \end{aligned}$$

$$R_{CMP} = \frac{(30 - 8 - 14) \times 270 \times (2700 + 300)}{\left(30 - 8 - \frac{2.4}{2} \times 7.2 \right) \times 0.87} = 447\Omega$$

In the formula, only the voltage loss of the flyback switch is taken into account, but there is also a small voltage loss in output stage B. To correct the calculated value that is a little bit too high, round off the value downwards by means of choosing the next lower value in the E-range. So: $R_{CMP} = 390k\Omega$.

So when a TV chassis used with different picture tubes with different $I_{o(p-p)}$ and R_{coil} , the value of R_{CMP} has to be adapted with each picture tube.

In fig 23, fig 24 and fig 25 are some oscilloscope pictures of an application, for different values of R_{CMP} . Pay attention to the differences in flyback time.

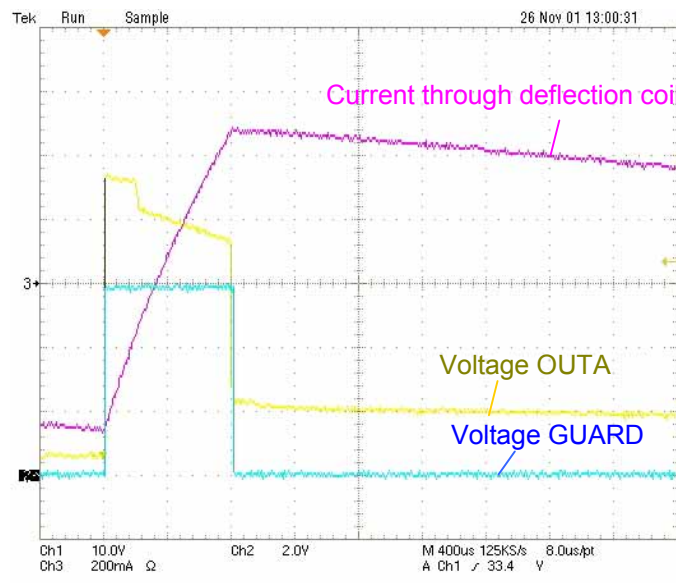


fig 23: Correct value of R_{CMP} .

In fig 23, the value of R_{CMP} is correct. The result is a correct waveform of the coil current, output voltage and the vertical guard. The flyback time is 800 μ s.

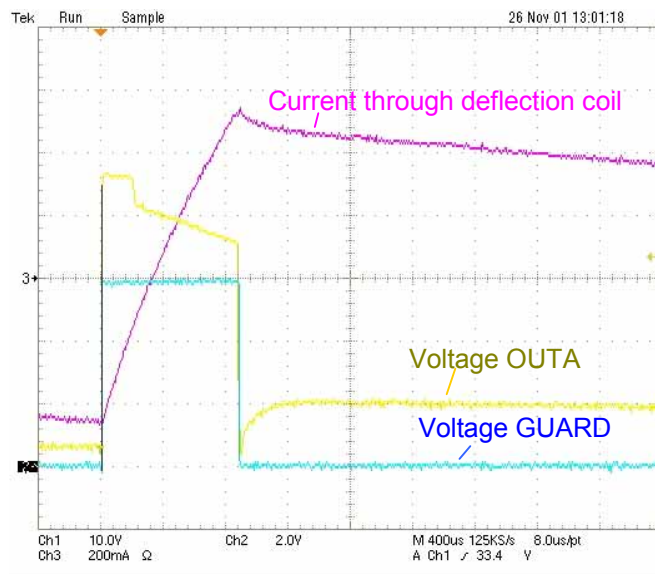


fig 24: R_{CMP} too low, current overshoot at start scan / end flyback, too much compensation.

In fig 24 the value of R_{CMP} is too low. The result is an overshoot condition in the output current and longer flyback time than in fig 22 (900 μ s). Also the active high time of the vertical guard is longer than in fig 22.

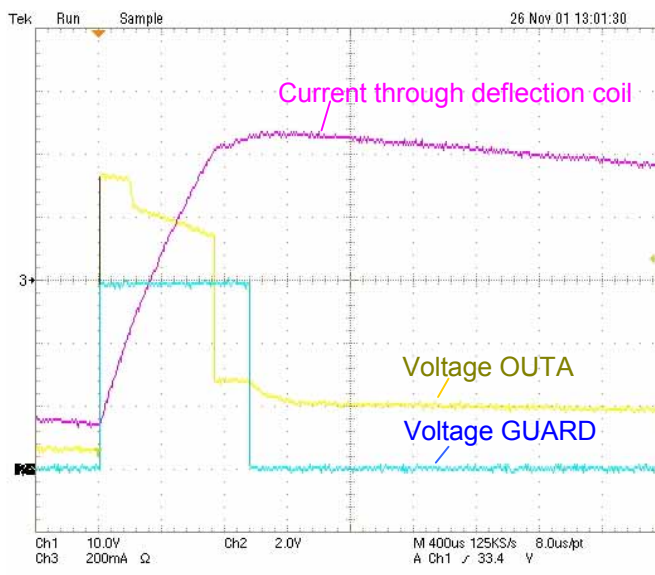


fig 25: R_{CMP} too high, current undershoot at start scan / end flyback, too less compensation.

In fig 25 the value of R_{CMP} is too high. The result is an undershoot condition in the output current and clipping of the output voltage to the supply voltage V_P . The output current has not yet reached the level as given by the input signal, this is similar to an open loop condition and the vertical guard remains high. So the active high time of the vertical guard is longer (1000 μ s).

Be aware that when R_{CMP} does not have the correct value, the vertical guard signal of pin 11 GUARD has a different active HIGH time in comparison with the flyback time.

2.9 Protection Circuits

The output circuit contains protection circuits for:

- Too high die temperature.
- Overvoltage of output A.

2.9.1 High die temperature

A temperature sensor is located on the die of the TDA8358J. If this sensor detects a temperature of approximately 170 °C, the protection circuit activates. The protection circuit reduces the drive of the output stage and the current through the coil is reduced. The guard output becomes high and can be used to signal the TV signal processor that a fault condition occurred.

2.9.2 Overvoltage output A

The overvoltage protection is activated, when the voltage of output stage A (pin 10 OUTA) increases above 70 Volt. During this condition, the protection circuit switches on MOSFET (M4) of output stage A, so M4 conducts and the output voltage at pin 10 OUTA decreases.

To prevent a short-circuit between pin 9 V_{FB} and pin 10 OUTA, at active overvoltage protection, the flyback switch M5 is prevented to conduct.

Output stage B is 'self-protecting' because if an over-voltage occurs at output stage B (pin 4 OUTB), the parasitic diode from the top MOSFET (M1), conducts and the current is led to the elco at pin 3 V_P . (This is not possible at output stage A, because diode D1 would block the current path to the elco at pin 3 V_P)

2.10 Vertical Guard Circuit

Pin 11 Guard

The TDA8358J has an internal vertical guard circuit, which delivers the guard signal to output pin 11 GUARD. This vertical guard circuit generates a pulse during every vertical flyback and at other conditions when the picture tube should be blanked. It can also be used to prevent the picture tube from burn-in, (due to faulty vertical deflection conditions) and as a vertical synchronisation signal to a microprocessor for e.g. On Screen Display. This guard pulse can be monitored by the TV signal processor.

The guard output is active (high) for one of the following conditions:

1. During the vertical flyback period.
2. During an open-loop condition of the TDA8358J. The circuit of the TDA8358J can see an open loop condition e.g. when the output voltage is clipping to the supply voltage V_P or clipping to the ground level due to a too low value of V_P or due to a too high value of the compensation resistor R_{CMP} .
3. During thermal protection of the TDA8358J (See section 2.9.1)

The guard output stage is a current source. In most applications a load resistor on pin 11 GUARD is used. This load resistor is used for having a quicker fall time of the guard pulse.

Be aware that when the compensation resistor R_{CMP} does not have the correct value or the value of the main supply voltage V_P is too low, the vertical guard signal has a different active HIGH time in comparison with the flyback time.

2.10.1 Vertical guard with TDA935X/6X/8X/N2 / TDA955X/6X/8X family as TV signal processor circuit.

2.10.1.1 Pin BLKIN of TV signal processor

In the TDA935X/6X/8X and TDA955X/6X/8X family the vertical guard function can be combined with the black current measuring input, pin BLKIN. For a reliable operation of the protection system and to avoid that the black current stabilisation is disturbed, the end of the vertical guard pulse should not overlap the RGB measuring pulses. Therefore this guard pulse must end before the black current measurement line. **Taking a higher flyback supply voltage V_{FB} is a way to make the guard pulse width smaller.** Or see section 2.10.1.3

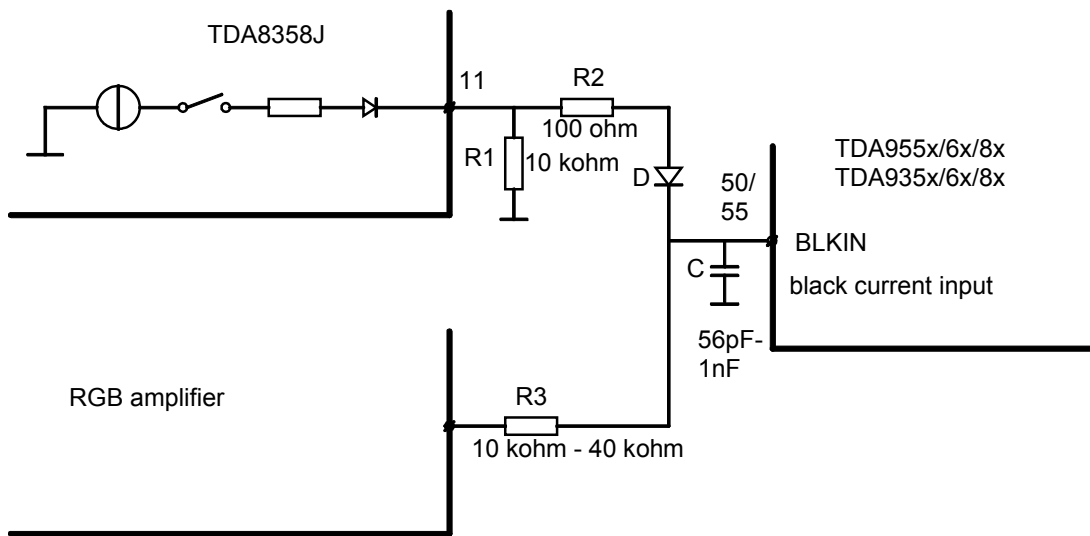


fig 26: Guard application for TDA955X/6X/8X / TDA935X/6X/8X family

In fig 26 is given the application for connecting the guard to the TDA955X/6X/8X / TDA935X/6X/8X family. Pin 11 GUARD of the TDA8358J is connected to pin 55/50 BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family. The black-current measurement output of the RGB-amplifier is also connected to pin 55/50 BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family.

Load resistor R1 is used for optimising the fall time of the guard pulse. The value of R1 is 10kΩ.

When pin 11 GUARD is connected to BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family and the load resistor R1 is used, the black current measurement pulse is disturbed by R1. After the guard interval the TDA955X/6X/8X / TDA935X/6X/8X family starts the black level setting by measuring the leakage current. When this leakage current is measured, no extra load must be seen. So a diode D in series must be used for isolating the load resistor.

In fig 27 a scope picture of an application, which uses the guard function on pin BLKIN, is given. The TDA9587H is used as TV signal processor circuit.

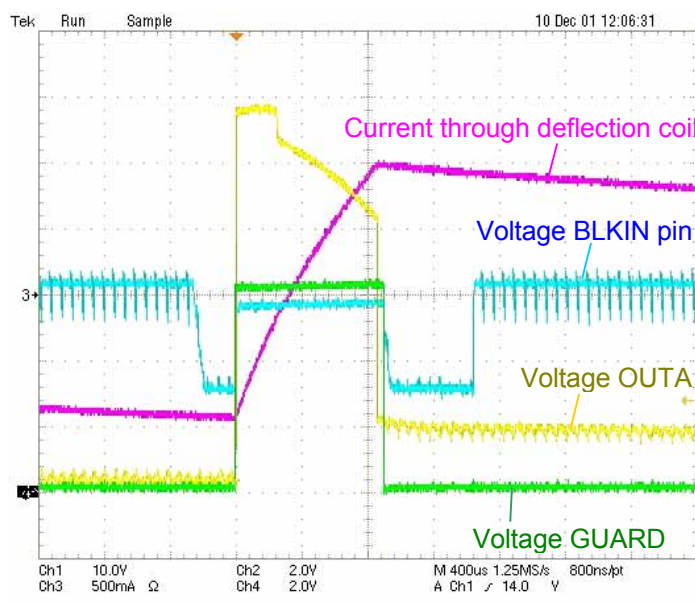


fig 27: Scope picture of application with vertical guard on BLKIN.

2.10.1.2 Pin BCLIN of TV signal processor

In the TDA935X/6X/8X and TDA955X/6X/8X family the vertical guard function can also be combined with the beam current limiting input, pin BCLIN.

When pin 11 GUARD is connected to BCLIN of the TDA935X/6X/8X and TDA955X/6X/8X family and a load resistor of 10 - 12kohm is used, the beam current limiting circuit is disturbed. So a diode in series must be used for isolating the load resistor.

2.10.1.3 Smaller vertical guard width

For a reliable operation of the protection system and to avoid that the black current stabilisation is disturbed, the end of the vertical guard pulse should not overlap the RGB measuring pulses. When the flyback pulse is too long, the circuit of fig 28 can be used to make the vertical guard pulse width smaller. See fig 29 for the result of the circuit of fig 28.

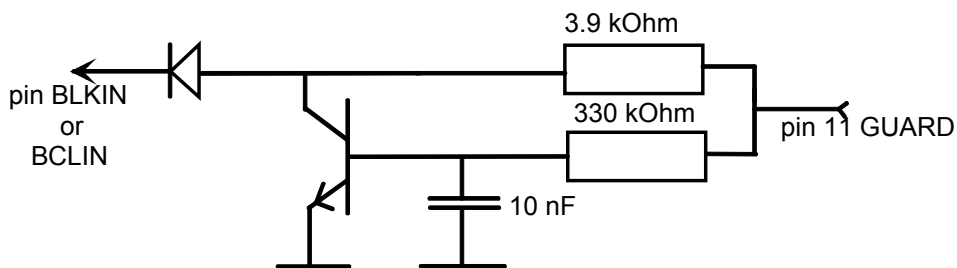
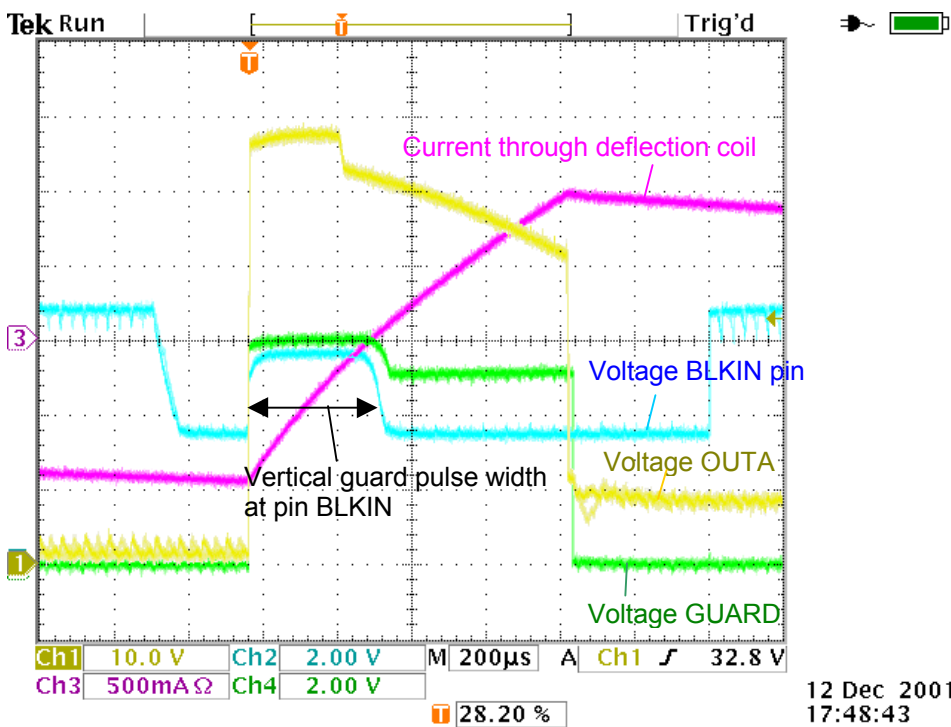


fig 28: Circuit for smaller vertical guard pulse width



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fig 29: Small vertical guard pulse width

2.10.2 Vertical guard with TDA884X/5X family as TV signal processor circuit.

The TDA884X/885X family or other TV signal processor circuits can monitor the guard output, which generates a pulse. Whenever the height of this pulse is larger than 3.65 V and the DC-level is correct the vertical deflection device works correctly. However for the TDA884X/885X family during scan the DC level may decrease below the 3.65 V level. Any other waveform is considered as failure and leads to blanking of the RGB outputs (see fig 30.)

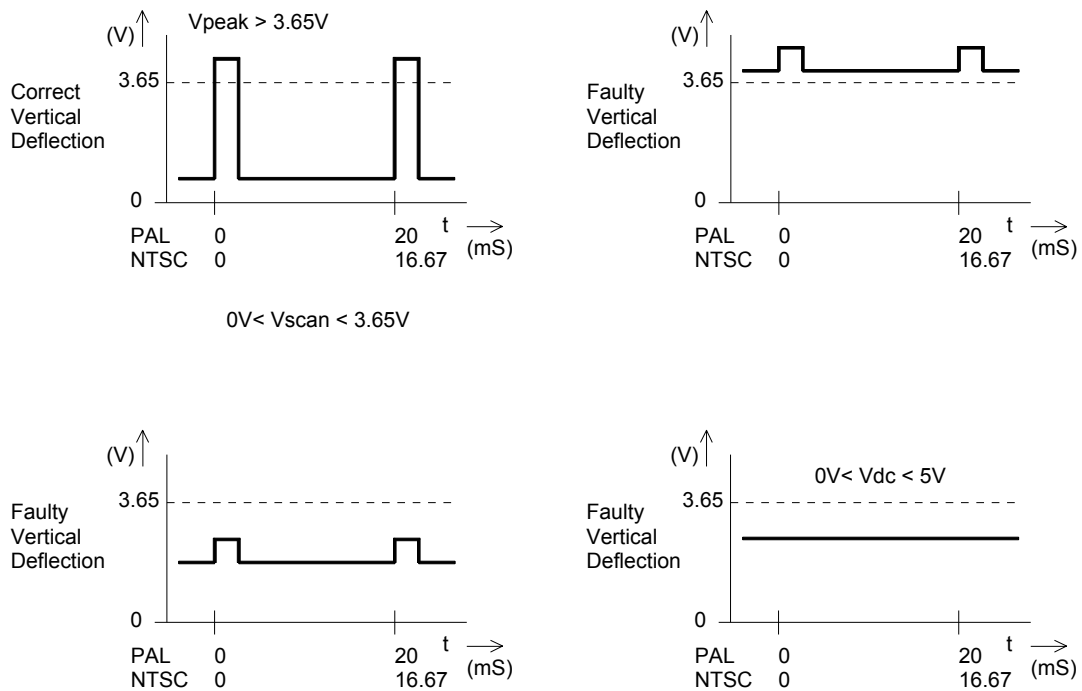


fig 30: Guard pulses with TDA884X/5X family

2.10.2.1 Vertical guard pulse connection with beam current limiting.

The beam current limiting function is realised by reducing the contrast followed by the brightness when the beam current reaches a too high level. The circuit can be divided into:

- Peak white limiting (PWL): reacts internally on high local peaks of the RGB signal
- Average beam current limiting (ABL): reacts on the average picture content. It is an external function.

In the next figure an application diagram is given which combines the two-beam current limiting functions (PWL and ABL) of a TDA884X/5X family device with the vertical guard function of the TDA8358J.

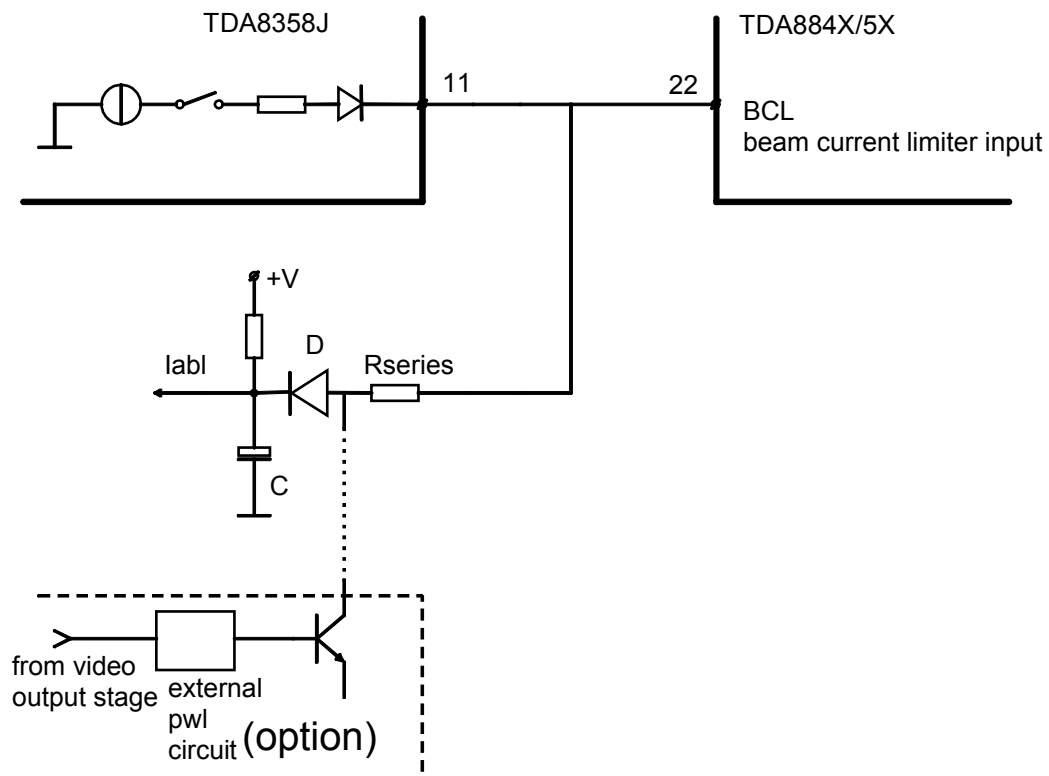


fig 31: Guard with beam current application

The combined input of the TDA884X/885X family has the following characteristics:

- * If the BCL is not active the voltage on pin 22 is 3.3 Volts, or higher.
- * When BCL is active the internal impedance of pin 22 is 40 kOhm.
- * The current that has to be pulled out the BCL-pin is constant.
(Approximately 40µA) over the whole range.

The diode D in series has two functions:

- * preventing that the voltage at pin 22 can be driven above 3.65 Volts that can disturb the vertical guard function.
- * Isolating pin 22 from capacitor C in order to ensure a fast PWL function of the TDA884X/5X family.

Important to know is that the BCL-circuit forms a load to the output signal of the vertical guard output circuit. This load should be below 1mA (at 4.5V pulse level). The min. series resistor at pin 22 can be calculated by:

$$R_{series} = \frac{V_{guard} - V_{c \min} - V_{fdiode}}{I_{guard \max}} = \frac{3.65V - 0V - 0.65V}{1mA} = 3k\Omega \quad V_{fdiode} \approx 0.65V$$

In this formula only the minimum voltage on the averaging capacitor is determined by the design of the ABL-function. (The minimum voltage on the averaging capacitor occurs at maximum beam current.)

In case $V_{c \min} = 0V$; $R_{series} = 3k$. It is wise to use a higher value as series resistor therefore in fig 31, a value of 5.6k as R_{series} has been chosen. Take also into consideration that in some applications $V_{c \min}$ can become negative.

2.10.2.2 Vertical guard pulse connection with high load (high current).

If the vertical guard pulse is also used as V-sync, take care that the maximum load is not exceeded. In this case it is possible to buffer first the vertical guard signal at the output of vertical deflection IC by means of a PNP-emitter follower. In order to separate the BCL-voltage on pin 22 from the buffered vertical guard (V-sync) signal, a diode D from the emitter of the PNP to BCL-pin should be added, otherwise the vertical guard signal used as V-sync information will be disturbed (see fig 32).

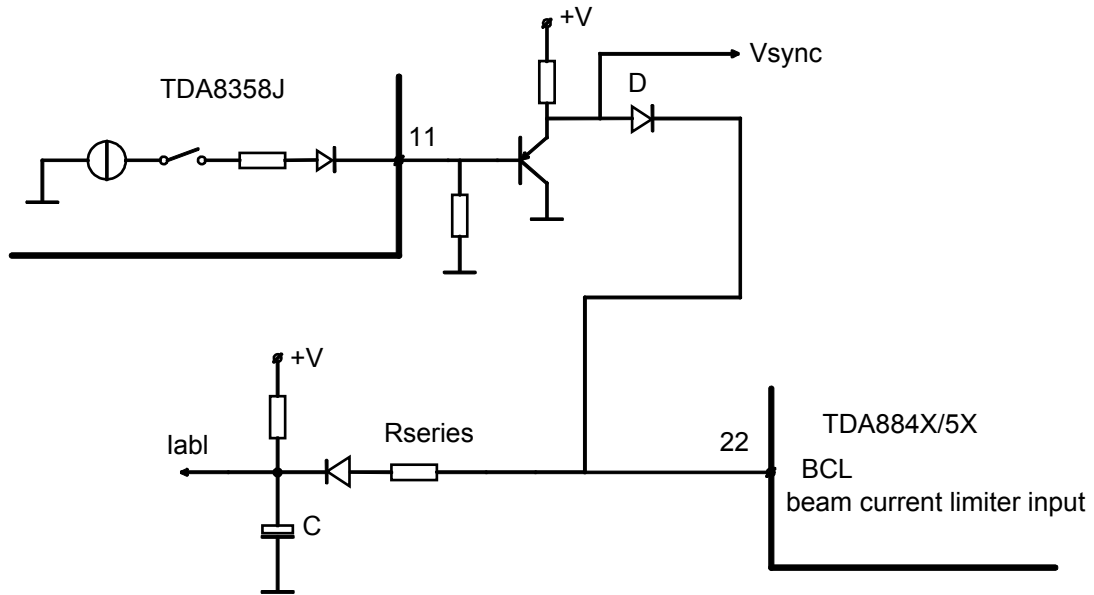


fig 32: Application for guard pulse with high load

2.11 Supplies

The TDA8358J concept has two power-supplies, a flyback supply and a main supply, which are calculated independently. The principle of operating with two supply voltages (class G) allows the use of an optimum main supply voltage V_P for scan and an optimum flyback supply voltage V_{FB} for flyback. This method achieves very high efficiency.

The TDA8358J has a good voltage supply ripple rejection. So in general a supply capacitor with a value of 220 μF will be sufficient for the main supply voltage V_P . This capacitor must be connected on pin 3 V_P . For the flyback supply voltage a supply capacitor connected on pin 9 V_{FB} with a value of 47 μF will be sufficient.

2.11.1 Calculation of the main supply V_P

Pin 3 V_P

There is a voltage drop across the coil during scan, which is determined by the coil impedance. The coil impedance exists of a resistive part and an inductive part so the total voltage drop across the coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign.

The internal output transistors have voltage losses. These voltage losses must be taken into account for calculation of the main supply voltage V_P .

The value of the internal voltage losses given by the output transistors can be found in the next graph (see fig 33). $V_{\text{loss}(1)}$ gives the voltage loss for the first part of the scan time. So $V_{\text{loss}(1)}$ is the sum of the voltage losses of MOSFET M2, diode D1 and MOSFET M3. $V_{\text{loss}(2)}$ gives the voltage loss for the second part of the scan time. . So $V_{\text{loss}(2)}$ is the sum of the voltage losses of MOSFET M1, MOSFET M4. See fig 12.

The difference of values between $V_{\text{loss}(1)}$ and $V_{\text{loss}(2)}$ is caused by the internal diode D1.

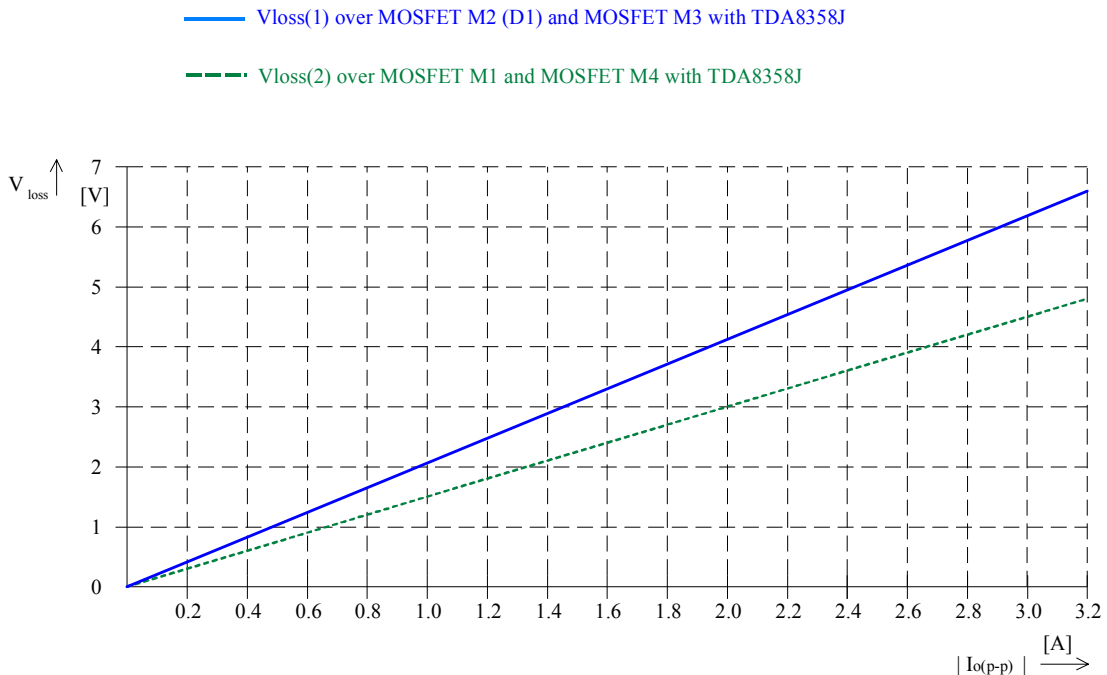


fig 33: Voltage loss of the output stage.

To calculate the minimum required supply voltage V_P , several specific application parameters have to be known:

- The peak to peak output current; $I_{o(p-p)}$
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; R_M
- The value of the deflection coil inductance; L_{coil}
- The value of the maximum vertical frequency; $f_{vert(max)}$
- $V_{loss(1,2)}$; see fig 33

The required power supply voltage V_P for the first part of the scan:

$$V_{P(1)} = \frac{I_{o(p-p)}}{2} \times (R_{coil(hot)} + R_M) - L_{coil} \times I_{o(p-p)} \times f_{vert(max)} + V_{loss(1)}$$

The required power supply voltage V_P for the second part of the scan:

$$V_{P(2)} = \frac{I_{o(p-p)}}{2} \times (R_{coil(hot)} + R_M) + L_{coil} \times I_{o(p-p)} \times f_{vert(max)} + V_{loss(2)}$$

Finally, after calculating the voltage supply by means of the above formulae, the minimum required value has to be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. This value has to be increased by 5% due to spread in the line output transformer and the deflection coil.

In the next example is shown how the main supply is calculated with TDA8358J:
We suppose the following:

$$\begin{aligned} I_{o(p-p)} &= 2.4 \text{ A} \\ R_{\text{coil}} &= 6 \Omega * 1.2 = 7.2 \Omega \\ R_M &= 0.87 \Omega \\ L_{\text{coil}} &= 5 \text{ mH} \\ f_{\text{vert(max)}} &= 50 \text{ Hz} \\ V_{\text{loss(1)}} &= 4.9 \text{ V (see fig 33)} \\ V_{\text{loss(2)}} &= 3.6 \text{ V (see fig 33)} \end{aligned}$$

First part of scan:

$$V_{P(1)} = \frac{2.4}{2} \times (7.2 + 0.87) - 5 \times 10^{-3} \times 2.4 \times 50 + 4.9 = 13.98V$$

Second part of scan:

$$V_{P(2)} = \frac{2.4}{2} \times (7.2 + 0.87) + 5 \times 10^{-3} \times 2.4 \times 50 + 3.6 = 13.88V$$

So we must choose 14 V and increase this value by 5% to get the minimum required supply voltage, $V_P = 14.7V$.

Be aware that when the value of V_P is too low, the vertical guard signal of pin 11 has a different active HIGH time in comparison with the flyback time. When the V_P is too low, The output voltage of pin 10 OUTA is clipping to the V_P at the beginning and end of the scan time. The circuit sees then an open loop condition and makes the vertical guard high.

2.11.2 Calculation of the flyback supply

Pin 9 V_{FB}

The flyback time is basically set by the value of the flyback voltage. So the flyback time can be optimised by choosing the appropriate flyback voltage. At the end of the flyback time, a settling time is needed at the start of the scan before the linear scan begins. Generally the settling time is covered by the overscan time. For the TDA8358J the settling time is nearly zero if the compensation resistor R_{CMP} has the correct value.

In a television application the value of the flyback time has to be shorter than the frame blanking time of the television standard. Mostly the flyback time starts half a line after the equalisation pulses. The flyback time must end before the generated measuring lines for the next frame. Generally in monitor applications a shorter time is needed, but that depends on the standard that is used.

In the next figure, the voltage across the coil during the flyback time is simplified as a voltage jump:

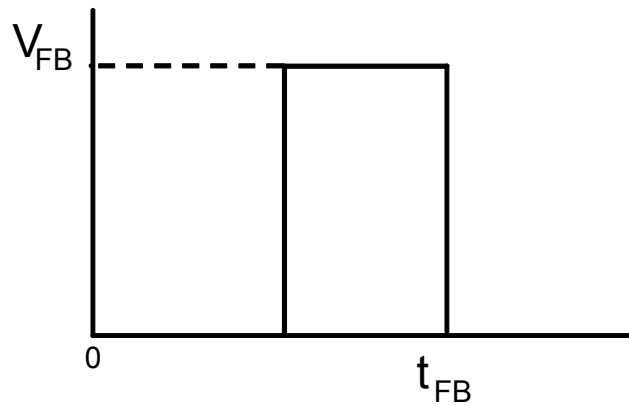


fig 34: Simplified flyback time.

To calculate the required supply voltage V_{FB} , several specific application parameters have to be known:

- The peak to peak output current; $I_{o(p-p)}$
- The maximum flyback current supply; $I_{FB(max)}$
- The flyback time; t_{FB}
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; R_M
- The value of the deflection coil inductance; L_{coil}

Using the simple model of fig 34, the flyback voltage V_{FB} is calculated by:

$$I_{o(p-p)} = I_{FB(max)} \times \left(1 - e^{-t_{FB}/x} \right)$$

Where: $I_{max} = \frac{V_{FB}}{R_{coil(hot)} + R_M}$ and $x = \frac{L_{coil}}{R_{coil(hot)} + R_M}$

$$\Leftrightarrow I_{o(p-p)} = \frac{V_{FB}}{R_{coil(hot)} + R_M} \times \left(1 - e^{-t_{FB}/x} \right)$$

$$\Leftrightarrow I_{o(p-p)} \times (R_{coil(hot)} + R_M) = V_{FB} \times \left(1 - e^{-t_{FB}/x} \right)$$

so :

$$V_{FB} = \frac{I_{o(p-p)} \times (R_{coil(hot)} + R_M)}{1 - e^{-t_{FB}/x}}$$

The simplified formula above assumes that the voltage during the flyback time is constant. Actually, in an application the flyback voltage is *not* constant during the flyback time. See also section 2.7. The influence of the damping resistor (R_{D1}) can be neglected.

Furthermore there is no need to increase the flyback voltage to compensate the spread in the line output transformer and the deflection coil, because the calculated flyback voltage is about 5% to 10 % *higher* than required and is settled when the formulas above are used.

In the next example is shown how the flyback supply is calculated with TDA8358J:
We suppose the following:

$I_{o(p-p)}$	= 2.4 A
$R_{coil(hot)}$	= $6 \Omega \times 1.2 = 7.2 \Omega$
R_M	= 0.87Ω
t_{FB}	= $640 \mu s$
L_{coil}	= 5 mH

then :

$$x = \frac{0.005}{7.2 + 0.87} = 619.6 \times 10^{-6}$$

$$V_{FB} = 2.4 \times \frac{7.2 + 0.87}{1 - e^{-\frac{640 \times 10^{-6}}{619 \times 10^{-6}}}} = 30.07V$$

So for the flyback supply voltage we choose 30 V.

2.12 East - West Amplifier**Pin 5 INEW, pin 8 OUTEW and pin 7 EWGND**

The TDA8358J includes an East - West amplifier. This E/W amplifier is current driven. The output can only sink currents from the diode modulator circuit. A feedback resistor R_{EWF} has to be connected between the input and output of this inverting amplifier in order to convert the E/W correction input current into an output voltage.

The output voltage V_{OUTEW} is:

$$V_{OUTEW} = I_{INEW} * R_{EWF} + V_{INEW}$$

The input circuit can be driven by drive circuits like TDA884X/5X (one chip family), TDA886X/7X/8X (bocma family), TDA935X/6X/8X and TDA955X/6X/8X (ultimate one chip family) and TDA485X (deflection processor family).

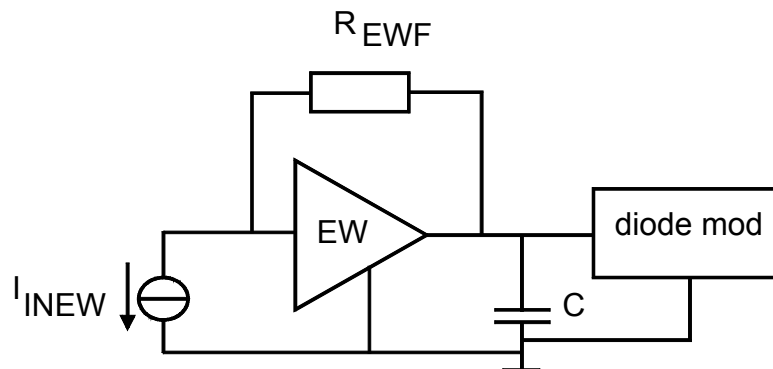


fig 35: Block diagram E/W

The maximum output voltage $V_{OUTEW(max)} = 68V$. This is the maximum voltage of the process in which the TDA8358J is made. The maximum output current $I_{OUTEW(max)} = 750mA$. The E/W amplifier is designed to sink output currents up to 750mA.

SOAR line of the East - West amplifier with different case temperatures:

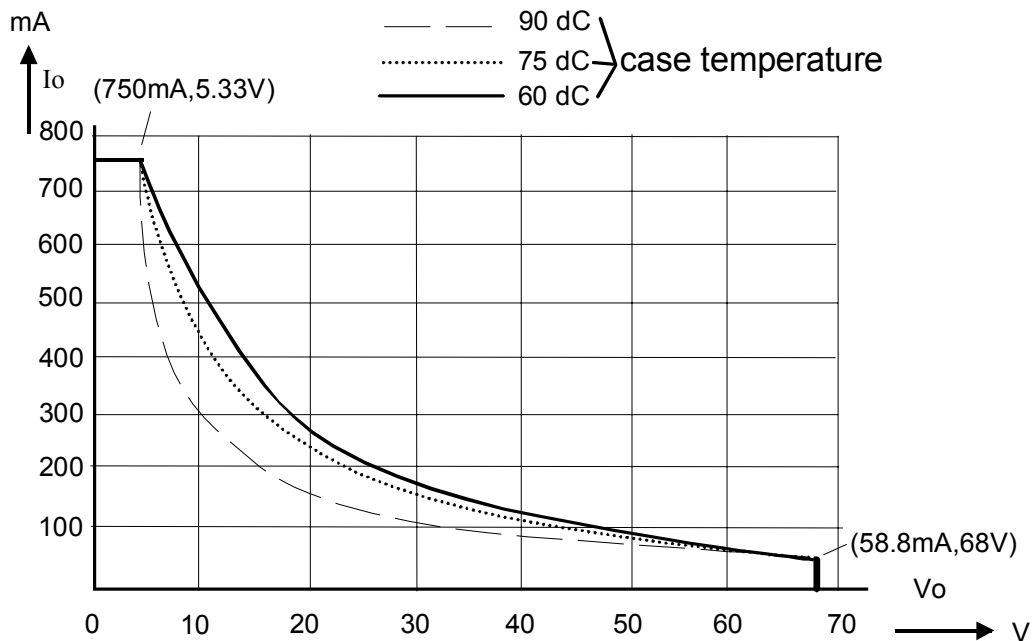


fig 36: SOAR line of East - West output stage

Operation outside the SOAR line is only allowed for a short time. Allowance is given for:

For a repetitive time duration of <0.1 ms the max. allowed peak dissipation is 15W. for a non repetitive time duration of <5 ms (set switch-on, set-switch-off) the max. allowed peak dissipation is also 15W.

At set switch on and while adjusting the picture width, the output current and /or the output voltage can be driven outside the SOAR region. Suppose the East - West width is set to minimum. This involves that the output current of the EW amplifier is zero and the DC voltage at the E/W amplifier pin is maximum. (max. allowed is 68 volt). Next the TV set is adjusted to its maximum width and consequently the E/W amplifier is driven to its maximum current. The output voltage being at maximum will decrease slowly due to discharge period of the loaded capacitor at the output pin. During this condition it is possible that the output load line crosses the SOAR line and can damage the output transistor. The excessive drive condition can be limited by taking the value of the series resistor R_{EWL} in the output as high as possible. The maximum value of R_{EWL} depends on whether in the TV signal processor the horizontal amplitude is still adjustable to the proper value.

2.12.1 Power calculation of the East - West stage.

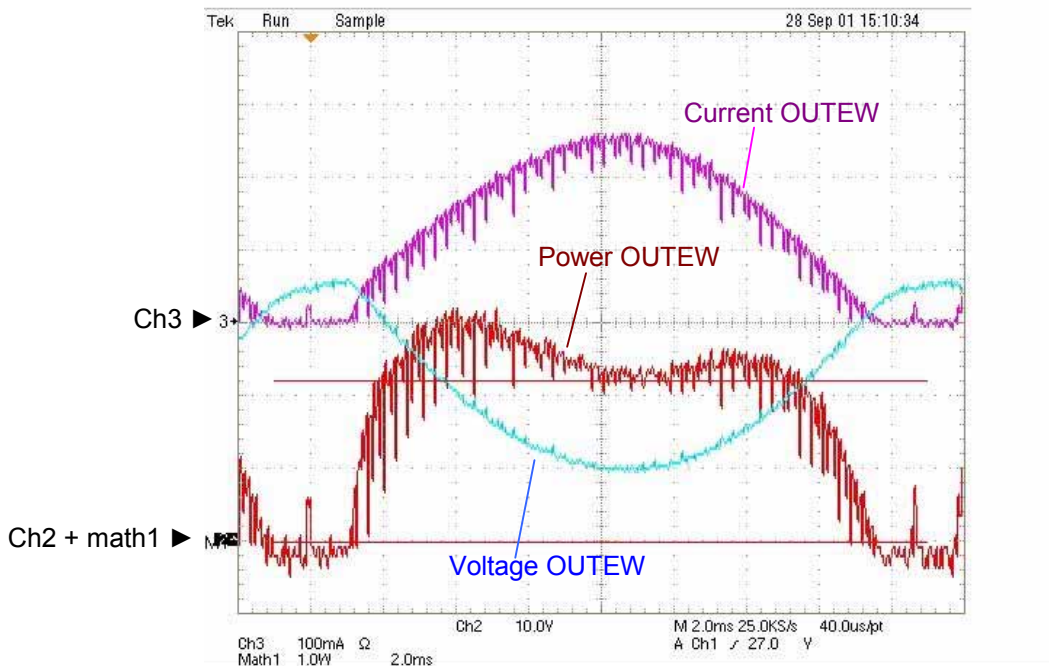


fig 37: Current, Voltage and power of pin 8 OUTEW

The shape of the East - West output pin 8 OUTEW waveform is in general a parabola. The output voltage will be higher at the beginning and end of the vertical scan compared to the voltage at the scan middle, while the output current will be higher at the scan middle. This results in an almost uniform power dissipation distribution during the vertical scan period. Therefore the power dissipation can be calculated by multiplying the average values of the output voltage of pin 8 OUTEW and the output current into pin 8 OUTEW.

$$P_{OUTEW} = V_{OUTEW(AV)} * I_{OUTEW(AV)}$$

When verifying the dissipation also the switch-on and switch-off dissipation should be checked. Power dissipation during these conditions can be 3 to 5 times higher than during normal operation.

2.12.2 Feedback resistor calculation.

The feedback resistor R_{EWF} can be calculated by:

$$V_{OUTEW} = I_{INEW} * R_{EWF} + V_{INEW}$$

If the input and output voltages and input current is known:

$$R_{EWF} = \frac{V_{OUTEW} - V_{INEW}}{I_{INEW}}$$

2.13 Heatsink calculation

The value of the heatsink can be calculated in the standard way with a method based on average temperatures. The required thermal resistance of the heatsink is determined by the maximum die temperature of 150° C. **However, in general we recommend designing for an average die temperature that does not exceed the 130°C.**

It should be noted that the heatsink thermal resistance $R_{th(h-a)}$ found by performing a standard calculation will be lower then normally found for a vertical stand alone device, due to the contribution of the E/W power dissipation to this value.

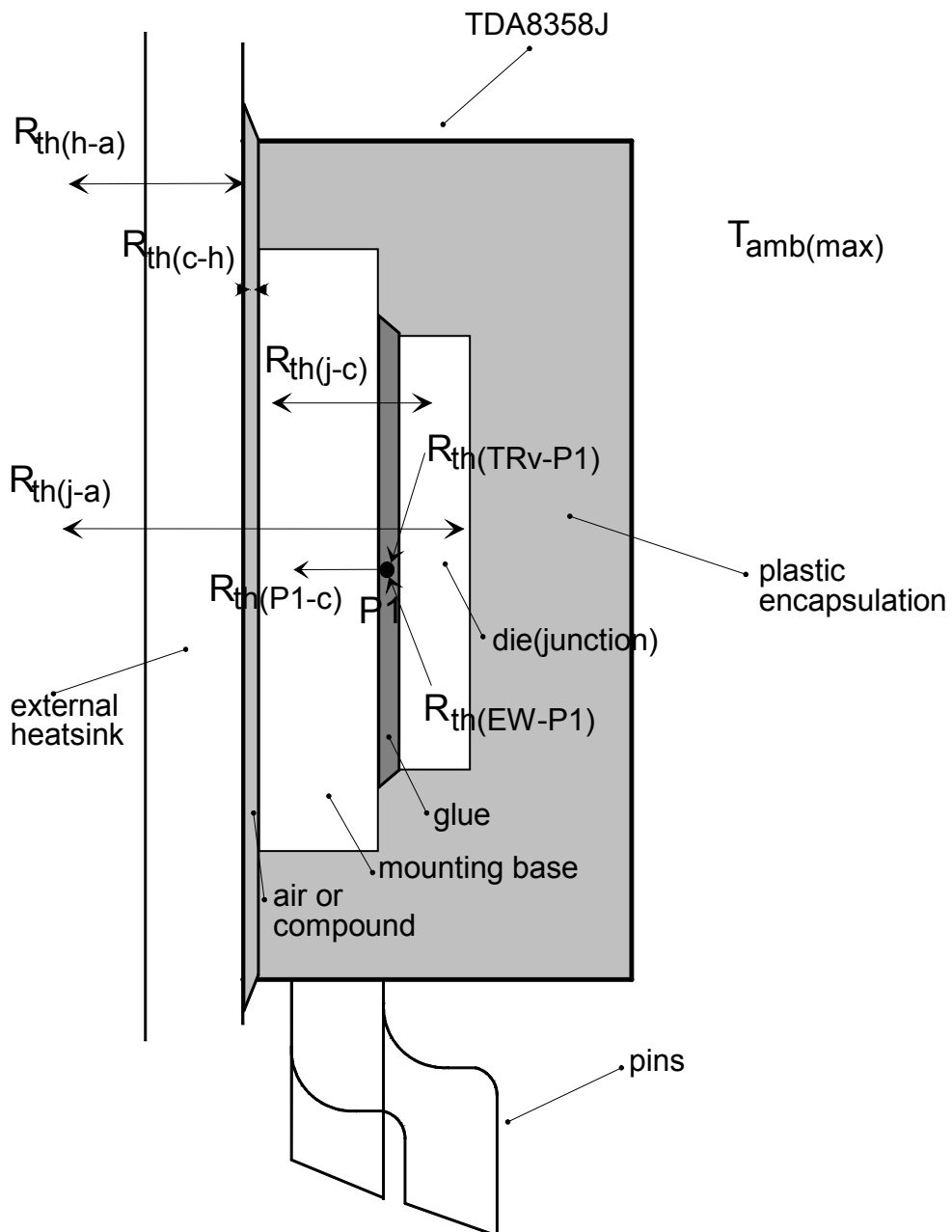


fig 38: Construction of TDA8358J mounted on a heatsink

The construction of the TDA8358J mounted on a heatsink is drawn in fig 38. In this picture several thermal resistances can be seen:

$R_{th(h-a)}$	= thermal resistance between heatsink and the ambient
$R_{th(c-h)}$	= thermal resistance between case (mounting base) and heatsink, depends on mounting method
$R_{th(j-c)}$	= thermal resistance between die (junction) and case (mounting base) = 4 K/W
$R_{th(j-a)}$	= thermal resistance between die and ambient
$R_{th(P1-c)}$	= thermal resistance between P1 and case (see 2.14.1)
$R_{th(TRv-P1)}$	= thermal resistance between TRv and P1 (see 2.14.1)
$R_{th(EW-P1)}$	= thermal resistance between EW and P1 (see 2.14.1)
$T_{amb(max)}$	= maximum ambient temperature

T_j	= temperature of the die (junction)
P_{tot}	= total power dissipation of the TDA8358J = $P_V + P_{EW}$
P_V	= power dissipation of the vertical output circuit (see 2.16)
P_{EW}	= power dissipation of the East - West circuit (see 2.12.1)

The thermal resistance $R_{th(j-a)}$ between the die and ambient is calculated by means of the next formulas:

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad \text{and} \quad T_j - T_{amb(max)} = P_{tot} \times R_{th(j-a)}$$

$$\Leftrightarrow T_j - T_{amb(max)} = P_{tot} \times (R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)})$$

$$\Leftrightarrow R_{th(h-a)} = \frac{T_j - T_{amb(max)}}{P_V + P_{EW}} - (R_{th(j-c)} + R_{th(c-h)})$$

The heatsink temperature T_h can be calculated:

$$T_h = T_{amb(max)} + (R_{th(h-a)} \times P_{tot})$$

Example of calculating $R_{th(h-a)}$ with TDA8358J:

Suppose:

T_j	=	130 °C (recommended maximum value)
$T_{amb(max)}$	=	40 °C
P_V	=	6 W
P_{EW}	=	3 W
$R_{th(j-c)}$	=	4 K/W
$R_{th(c-h)}$	=	1 K/W

$$R_{th(h-a)} = \frac{130 - 40}{6 + 3} - (4 + 1) = 5 \text{ K/W}$$

The heatsink temperature will be:

$$T_h = 40 + (5 \times 9) = 85^\circ\text{C}$$

It may be clear that, to *decrease* the temperature of the heatsink or the allowed temperature inside the cabinet, the dimensions of the heatsink should be *increased*.

It is recommended to check both output stages (vertical and East - West) on their individual contributions to the die temperature. It is possible to do this by using a thermal network, which is described in the next chapter.

2.14 Junction/die peak temperature check

The TDA8358J has two independent power dissipating circuits, the vertical output circuit and the East - West circuit.

It is recommended to verify the individual maximum (peak) junction temperature of both circuits. Therefore the maximum (peak) power dissipation of the circuits and also the heatsink temperature should be measured. The maximum (peak) junction temperatures can be calculated by using an equivalent thermal resistance network

2.14.1 Equivalent thermal resistance network.

A simplified resistor network can represent the thermal resistance:

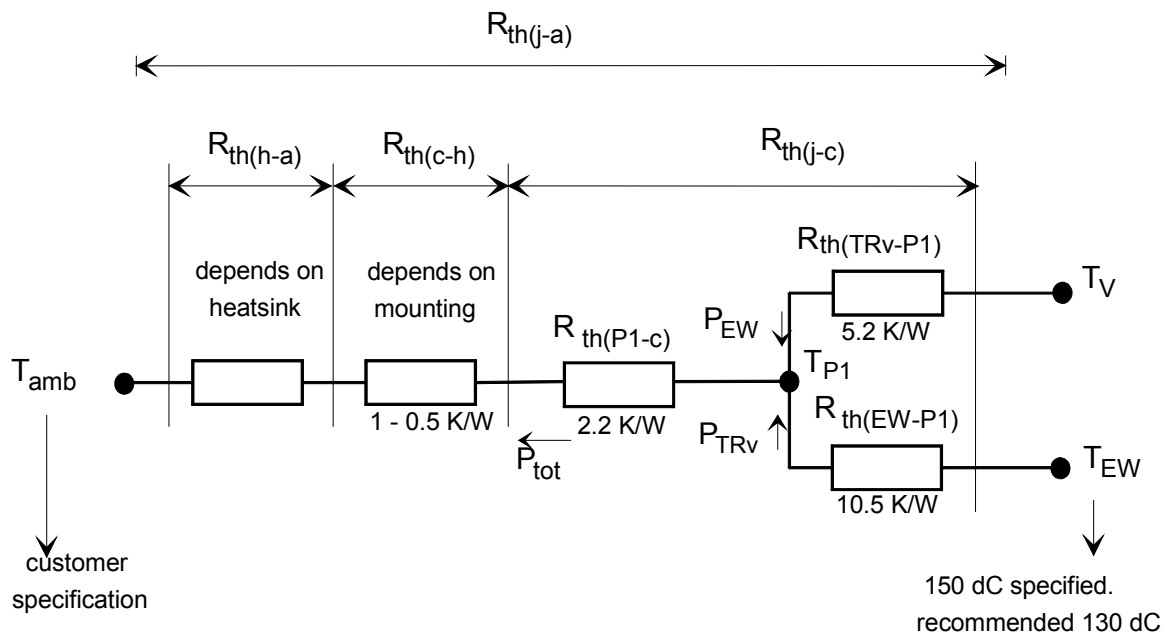


fig 39: Equivalent thermal resistance network

With the aid of a thermal simulation program the thermal behaviour is simulated and calculated. The temperature figures fed into the program have been measured in a standard application. Also the dissipated power in each part, vertical and East - West, have been measured and calculated in the same standard application. The results of the thermal simulation program were:

Thermal resistance of the $R_{th(TRv-P1)}$: 5.2 K/W

Thermal resistance of the $R_{th(EW-P1)}$: 10.5 K/W

Thermal resistance of the $R_{th(P1-c)}$: 2.2 K/W

The network does only include the contribution of the maximum (peak) power dissipation $P_{TRv(peak)}$, being the dissipation of the most critical transistor of the vertical output circuit, which is internally connected between pin 10 OUTA and pin 6 VGND. The model assumes equivalent maximum peak power dissipation during the different vertical scan stages for all the functionally paired transistors. The calculated maximum (peak) junction temperature T_j should not exceed 150 °C.

Point P1 is a virtual point inside the case. See fig 39.

The maximum (peak) temperature of point P1 $T_{P1(peak)}$ is given by:

$$T_{P1(peak)} = T_c + (P_{EW} + P_{TRv(peak)}) * R_{th(P1-c)}$$

T_c = temperature of the case (mounting base)
 P_{EW} = power dissipation of the East - West circuit
 $P_{TRv(peak)}$ = power dissipation of the most critical transistor
 $R_{th(P1-c)}$ = thermal resistance between P1 and case

The maximum (peak) junction temperatures for the output circuits are given by:

East - West: $T_{j(EW)(peak)} = T_{P1(peak)} + R_{th(EW-P1)} * P_{EW}$

$R_{th(TRv-P1)}$ = thermal resistance between TRv and P1

Vertical: $T_{j(TRv)(peak)} = T_{P1(peak)} + R_{th(TRv-P1)} * P_{TRv(peak)}$

$R_{th(EW-P1)}$ = thermal resistance between EW and P1

Calculating/Measuring $P_{TRv(peak)}$:

MOSFET M4 of the vertical output circuit is the most critical transistor, because it is the closest transistor to the East - West output transistor in the layout of the TDA8358J. See fig 40. Therefore MOSFET M4 becomes the hottest transistor of the vertical output circuit. So $P_{TRv(peak)}$ = the peak dissipation of M4.

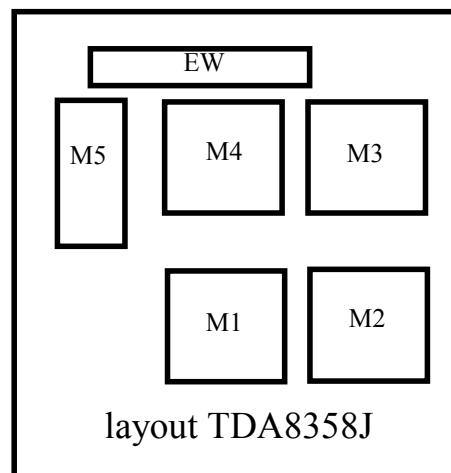


fig 40: Layout of both output circuits of the TDA8358J

With a digital oscilloscope the peak dissipation of M4 can be measured and calculated. M4, which is the bottom MOSFET of output A, is only active during the second half of the scan time together with M1, which is the top MOSFET of output B. See fig 41 and fig 42.

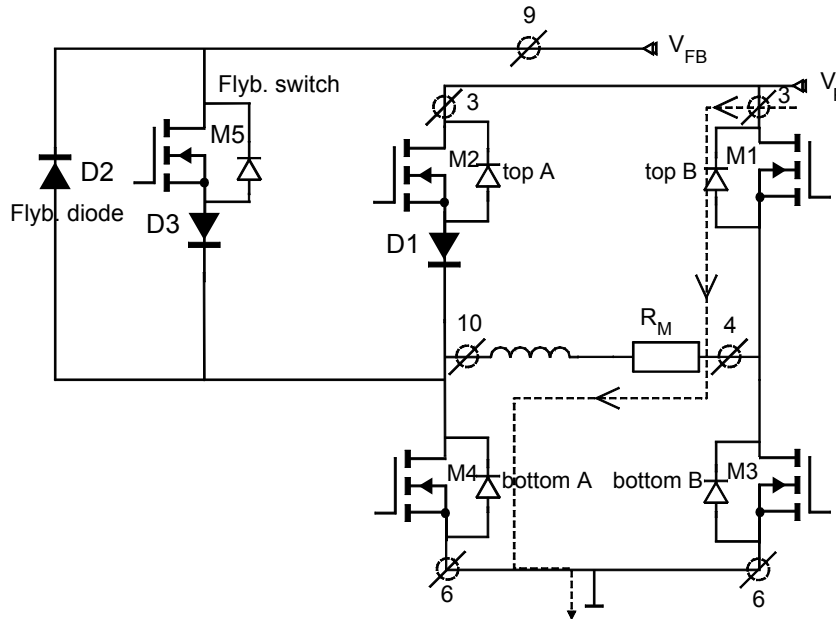


fig 41: Current path in second part of scan

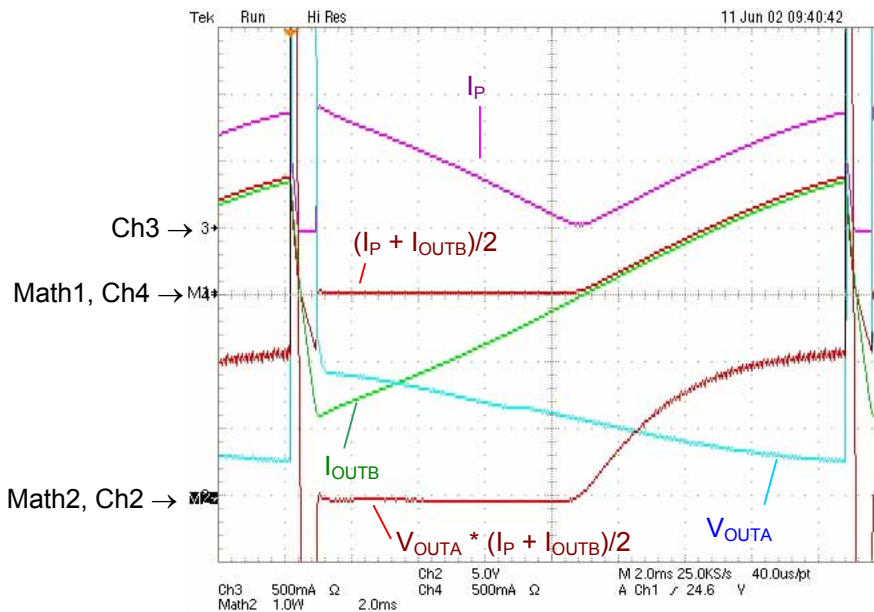


fig 42: Peak dissipation of M4

In this oscilloscope picture several waveforms can be seen:

- Ch2 = V_{OUTA} (blue) = measured voltage on pin 7 OUTA
- Ch3 = I_P (magenta) = measured current into pin 3 V_P
- Ch4 = I_{OUTB} (green) = measured current in wire from PCB to "B-side" of the vertical deflection coil
- Math1 = $(I_P + I_{OUTB})/2$ = calculated value by oscilloscope
- Math2 = $V_{OUTA} * (I_P + I_{OUTB})/2$ = calculated power dissipation of M4

During the second half of the scan time, I_P has nearly the same value as I_{OUTB} . However in the first part of the scan, I_P has the opposite value of I_{OUTB} . Therefore when those values are added and then divided by factor 2, the oscilloscope shows only the current value through M4 during the second part of the scan time. Now the power dissipation of M4 during the second half of the scan can be calculated and the peak power dissipation can be determined.

Calculating/Measuring P_{EW}

While M4 is only dissipation during the second half of the scan time, the peak temperature of the junction will be reached in the second half of the scan. So only the average power dissipation of the E/W output transistor P_{EW} during the second half of the scan time must be taken into account. P_{EW} during the second half of the scan time can be measured/determined with an oscilloscope. See fig 37.

Example of calculating $T_{j(EW)(peak)}$ and $T_{j(TRV)(peak)}$:

Suppose:

P_{EW}	= 3W (average during second half of scan time)
P_V	= 6W
$P_{TRV(peak)}$	= 5W
T_c	= 85°C

The maximum (peak) temperature $T_{P1(peak)}$ is given by:

$$T_{P1(peak)} = 85 + (3 + 5) * 2.2 = 102.6^{\circ}C$$

The maximum (peak) junction temperatures for the output circuits are given by:

$$T_{j(EW)(peak)} = 102.6 + 10.5 * 3 = 134.1^{\circ}C$$

$$T_{j(TRV)(peak)} = 102.6 + 5.2 * 5 = 128.6^{\circ}C$$

2.15 SOAR behaviour output

The TDA8358J is designed in a 68-volt LVD MOS (Low Voltage DMOS) process. The advantage of using MOSFETs instead of bipolar transistors for the output stage is the absence of second breakdown. fig 43 shows the Safe Operating Area of a bipolar transistor and of a MOSFET. It shows that the bipolar transistor delivers less current than the MOSFET, at a certain voltage. So a MOSFET output stage is more robust than a bipolar output stage. The restrictions for temperature are the same as those in the bipolar process.

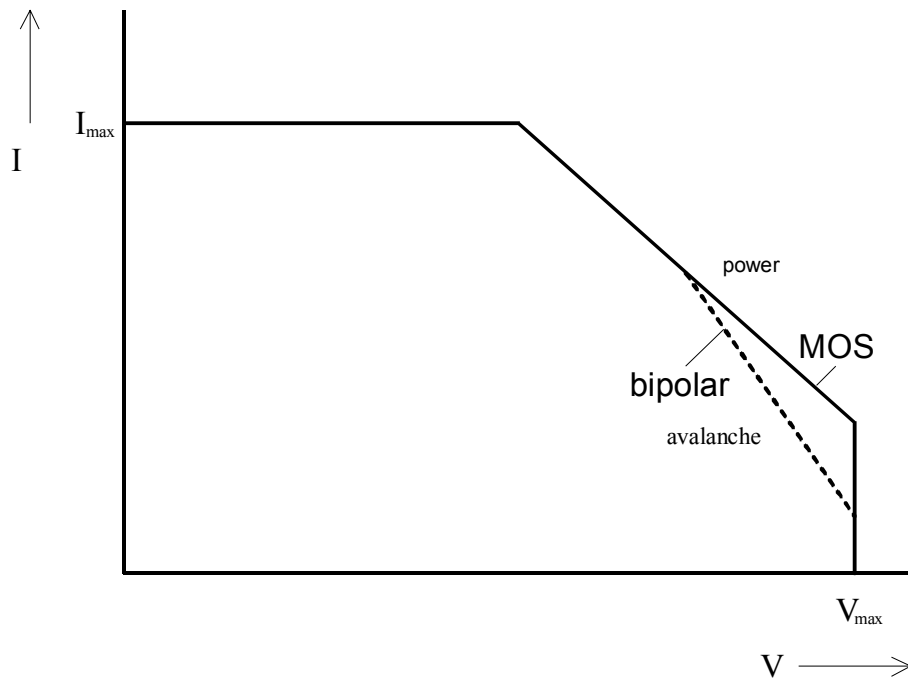


fig 43: Power limitations.

2.16 Power dissipation of the vertical output stage

The principle diagram of the bridge output stage is given in fig 44.

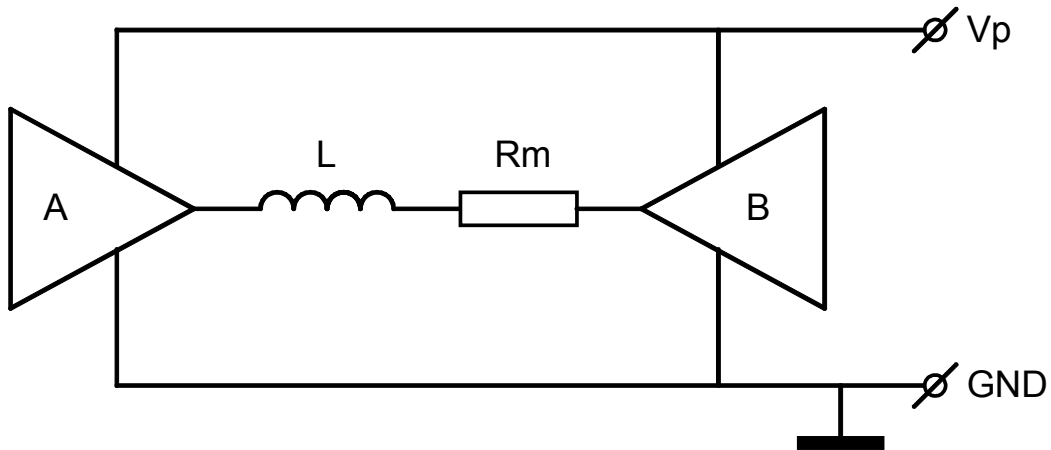


fig 44: Principle diagram.

The total power dissipation of the TDA8358J is given by the formula:

$$P_{\text{tot}} = P_{\text{sup}} - P_{\text{L}}$$

where:

P_{sup} = Power delivered by the supply

P_{L} = Power dissipation of the load that consists of $R_{\text{coil(hot)}} + R_{\text{M}}$

$R_{\text{coil(hot)}}$ = The value of the deflection coil resistance in hot condition = $R_{\text{coil(cold)}} \times 1.2$

R_{M} = The value of the measuring resistor

2.16.1 Power P_{sup}

The power that is delivered by the supply is calculated by means of the next formula:

$$P_{\text{sup}} = \frac{V_P \times I_{\text{sup(peak)}}}{2}$$

$$\text{or } P_{\text{sup}} = \frac{V_P \times I_{o(p-p)}}{4} \quad \text{because} \quad I_{\text{sup(peak)}} \approx \frac{I_{o(p-p)}}{2}$$

Where:

$I_{o(p-p)}$ = The peak to peak output current

V_P = Voltage of the main supply

The explanation of the formula is described, step by step, in the Appendix (section 4).

The power that is delivered by the quiescent current of the TDA8358J must also be taken into account:

$$V_P \times I_{q(p)}(av) = V_P \times 0.015$$

The contribution of the power during the flyback time is approximately 0.3W. This is an average value for the losses in the flyback supply.

So:

$$P_{\text{sup}} = \frac{V_P \times I_{o(p-p)}}{4} + V_P \times 0.015 + 0.3$$

2.16.2 Power dissipation P_L

The power that is dissipated by the load ($R_{\text{coil}} + R_M$) is calculated by means of the next formula:

$$P_L = \frac{I_{o(p-p)}^2 \times (1.2 \times R_{\text{coil}} + R_M)}{12}$$

The explanation of the formula is described, step by step, in the Appendix (section 4).

2.16.3 Total power dissipation P_{tot}

Eventually the total power dissipation of the TDA8358J is calculated by:

$$P_{\text{tot}} = P_{\text{sup}} - P_L = \left[\frac{V_P \times I_{o(p-p)}}{4} + V_P \times 0.015 + 0.3 \right] - \left[\frac{I_{o(p-p)}^2 \times (1.2 \times R_{\text{coil}} + R_M)}{12} \right]$$

Example of calculating P_{tot} with TDA8358J:

Suppose:

$$\begin{aligned} V_P &= 14.7\text{V} \\ I_{o(p-p)} &= 2.4\text{A} \\ R_{\text{coil}} &= 6\Omega \text{ (in cold condition)} \\ R_M &= 0.87\Omega \end{aligned}$$

$$P_{\text{tot}} = \left[\frac{14.7 \times 2.4}{4} + 14.7 \times 0.015 + 0.3 \right] - \left[\frac{2.4^2 \times (1.2 \times 6 + 0.87)}{12} \right] = 9.34 - 3.87 = 5.47\text{W}$$

2.17 Flash-over.

Flashover is a random phenomenon at which the energy stored in the aquadag capacitor of the picture tube is discharged by a current that rushes through the electrodes of the CRT to find a way from inner to outer aquadag.

Loose conducting particles or whiskers on metal parts of the grids and cathodes cause flashes. Usually it finds first the focus grid. But a flash may also travel along the glass surface inside the neck, to exit at the socket of the picture tube. Thus, by means of one of these routes a flashover may reach every pin on the tube base. While the number of discharges varies from electrode to electrode, none of them are completely free from flashover. Extensive precautions are taken at manufacturing of the picture tube.

Furthermore, for soft-flash CRT, a high ohmic inner conductive coating reduces the peak flashover current to about a tenth of the value of that for hard-flash CRT. Nevertheless flashes may still occur. Sparkgaps and series resistors to the gun electrodes are required as primary safeguards. In the application of the vertical deflection amplifier one must pay attention to a proper PCB layout.

2.17.1 Flash-over simulation

- The flash behaviour of a set can be simulated by means of a flash-mill.
- A flash mill consists of two brass ball electrodes, separated by a quartz disc.
- The disc provided with a hole rotates periodically by a motor between the pair of brass ball electrodes. When the hole is near the electrodes, a spark will jump between.

One wire of the flash-mill is connected to the EHT and the other is connected to the VG2 pin or the focus pin of the picture tube without series resistor.

2.17.2 Flashover behaviour of TDA8358JN2

The TDA8358JN2 has improved robustness of the internal low substrate leakage current diodes against flashover by construction and a new process. Evaluation in several customer sets with only a small RC-filter ($47\text{nF} + 1.5\Omega$) from pin 10 OUTA to pin 6 VGND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during flash testing on critical pins like focus and VG2.

From our experiences with flashover and other overstress testing in the past it is recommended, see fig 45:

- HF decoupling capacitors of the supplies V_P and V_{FB} must be close to pins of the IC in the PCB-layout. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 6 VGND. Avoid ground loops in the PCB-layout.

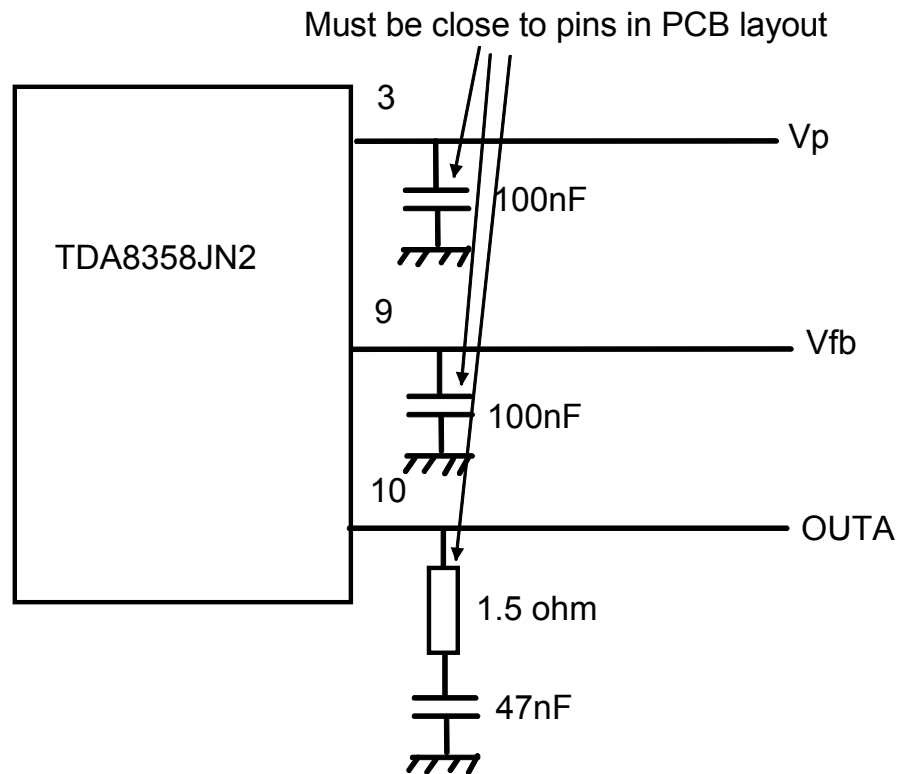


fig 45: Recommended layout for flashover protection

2.18 ESD-gun test

Next to the standard ESD-test on the TDA8358J (Human Body Model and Machine Model), another ESD-test is introduced by some customers. This ESD-test is introduced to test the application, which the TDA8358J is used in. This ESD-test is carried out by a standard ESD-gun, which is discharged on the connections of the vertical deflection coil mounted on the neck of the picture tube. The standard ESD-gun is discharged with a capacity of 150 pF and a series resistor of 330 Ω . This capacitor and resistor are standard IEC1000-4-2 (IEC 801-2, 1991) and are inside of the ESD-gun.

With the TDA8358JN1, some external components were needed for a better ESD-gun test behaviour. The TDA8358JN2 has improved robustness of internal low substrate leakage current diodes against overstress behaviour by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5 Ω) from pin 10 OUTA to pin 6 VGND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during ESD-gun testing up till 16.5 kV air discharge and 9kV contact discharge. These values (16.5 kV air discharge and 9kV contact discharge) are the maximum values of the NSG 435 ESD-gun.

From our experiences with ESD-gun testing in the past it is recommended:

- HF decoupling capacitors of the supplies V_P and V_{FB} must be close to pins of the IC in the PCB-layout. When the HF decoupling capacitor of the flyback supply V_{FB} is not close to the pin V_{FB} , the robustness is much lower. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 6 VGND. Avoid ground loops in the PCB-layout.

2.19 EMC behaviour

When problems are found around the EMC behaviour of the application, the problems should be split into:

1. Susceptibility problem (radiation coming from outside of the IC).
2. Radiation problem (coming from the IC itself).

In both cases it is important to know the frequency that causes the problem(s).

Recommendations:

Reduction of the susceptibility and radiation can be achieved by:

- limit the bandwidth of the system.
- keep loop areas small to reduce magnetic pick up.
- keep sensitive tracks short to reduce electrical pick up.

A. Bandwidth of the noise

The bandwidth can be limited by filtering the input, output and power supply. Pay attention to small loop areas and short tracks during the design of the layout of the printed circuit board.

B. Drive signal

The drive signal tracks from the drive circuit to the TDA8358J should be routed close to each other and made as short as possible. This is to minimise the loop area.

To suppress (EMC) interference it is possible to insert a series resistor of $100\Omega - 1k\Omega$ in the drive signals close to the TV signal processor. Furthermore capacitors can be used on the pins of the TV signal processor with a value of $560pF - 1nF$. In general, the use of small decoupling capacitors of $2.2 nF$ between the input pins and ground will solve problems at the input side. The capacitors must be connected directly to ground (pin 5) of the TDA8358J. This has to be done with short wires and tracks in order to minimise parasitic inductance.

C. Power supplies

It is recommended to decouple the power supplies locally and as close as possible to the TDA8358J. Especially the high frequency decoupling capacitor must be connected as close as possible to the pins of the IC. The main power supply and the flyback power supply, should be both decoupled with $100nF$ capacitors.

D. Deflection coil

The connection to the deflection coil is usual done with relatively long wires. These 'long' wires behave as an aerial, which picks up RF disturbances. If two blocking inductors of $2 \mu H$ are placed in these wires, a good blocking of the disturbance is achieved. The inductors can be implemented as a "bead on wire".

E. Heatsink

For good EMC behaviour the heatsink should be grounded and not left electrically floating. The copper backside of the TDA8358J is glued to the backside of the crystal and must be connected to the ground pin (pin 6 VGND).

F. Circuit

For optimal suppression, the circuit in fig 46 can be used as guidance.

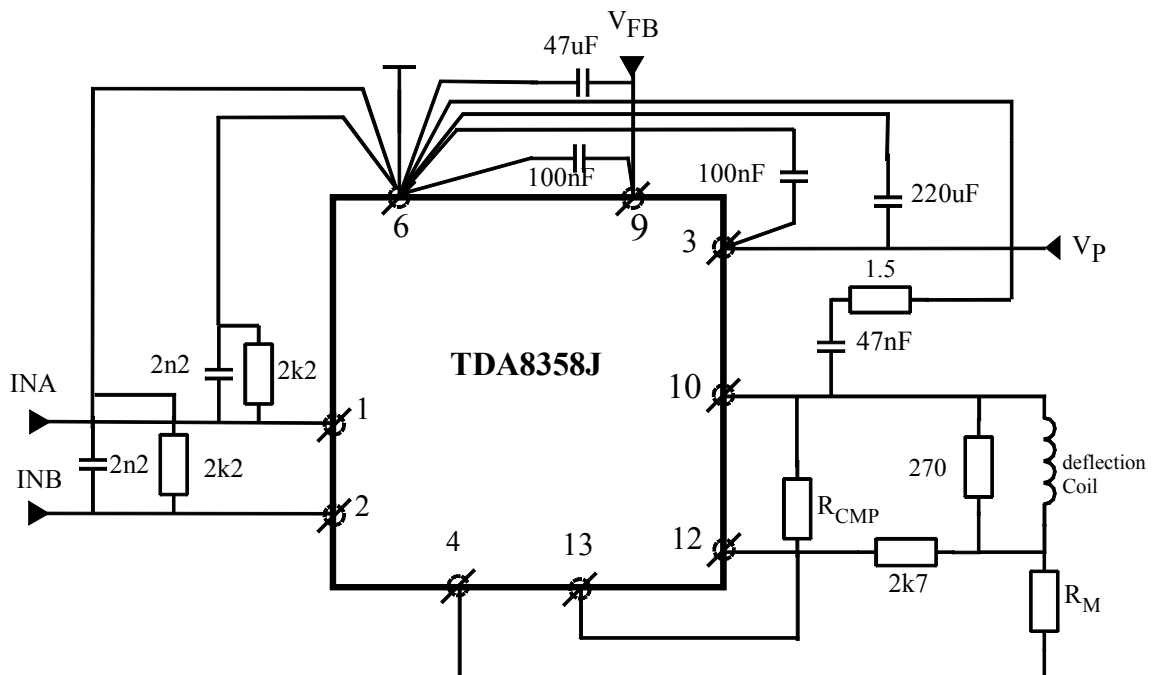


fig 46: Recommended application for optimal suppression.

2.20 Improved temperature coefficient in TDA8358JN2

The TDA8358JN2 has an improved temperature coefficient. A small layout modification is made in the TDA8358JN2, which reduces the temperature influence of the vertical amplitude. This temperature influence is checked in a customer TV-application. The picture height of the picture tube used is 410 mm. The results found are that the temperature influence of the vertical amplitude is reduced by a factor of 2.

2.21 Vertical compressed scan with TDA8358J

Vertical compressed scan is used in double window applications on 16:9 picture tubes and for the display of a 16:9 picture on a 4:3 picture tube. When vertical compressed scan is used with the TDA935X/6X/8X / TDA955X/6X/8X family ($V_X = 0$, $OSVE = 1$) the black current measuring lines are written in the vertical overscan. These measuring lines are written in the vertical overscan during the last four lines of the vertical flyback period. After the last line is written the vertical drive signal jumps to the starting point of the video lines. At this moment the output signal of the TDA8358J cannot follow the fast changing input signal, which forces the TDA8358J into an open loop condition. See fig 47.

This can be prevented by using a zener diode from pin 4 OUTB to pin 6 VGND. See fig 48. The zener diode prevents the output of the TDA8358J to be clipped to the supply voltage. The value of the zener diode has to be between the supply voltage V_P (about 2V lower) and the maximum output voltage on pin 4 OUTB (about 1 V higher). The zener diode must have low internal resistance and must be able to consume a peak current of about 2A, to assure proper operation.

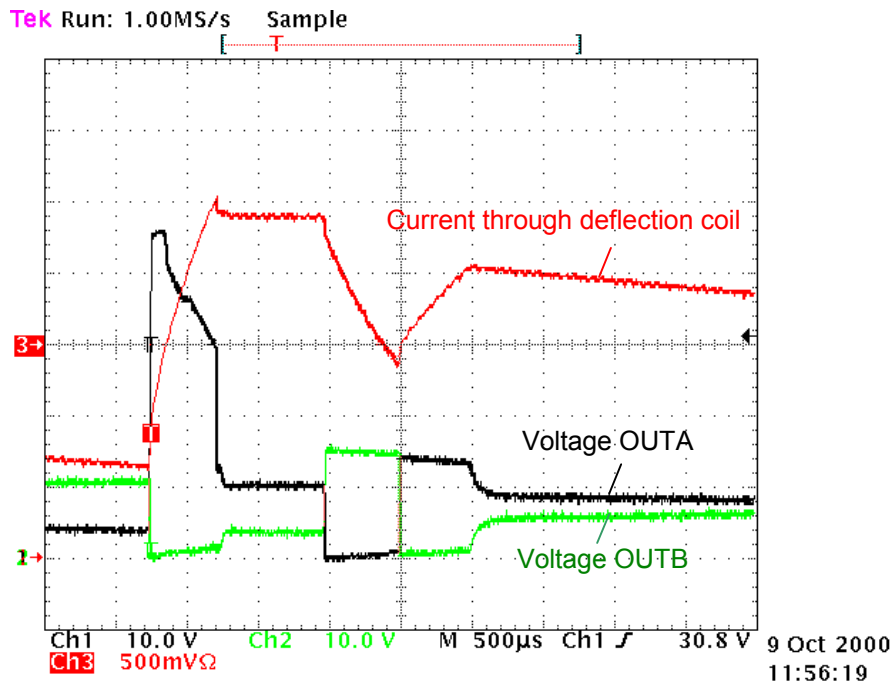


fig 47: Vertical compressed scan with TDA8358J

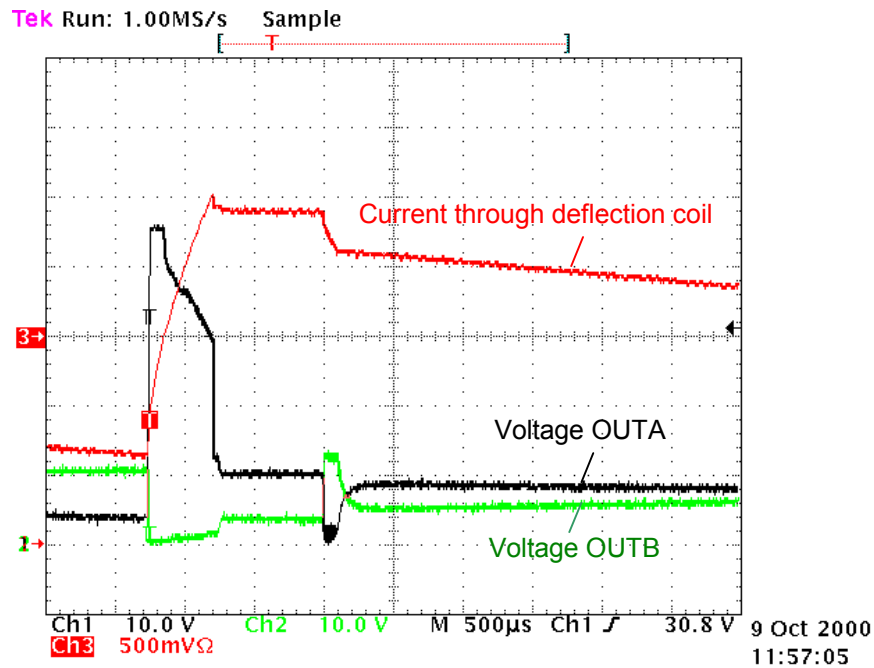


fig 48: Vertical compressed scan with TDA8358J with a zener diode on pin 4 OUTB to GND

2.22 Application design procedure of the TDA8358J.

Below is explained how to start with a design-in of the TDA8358J.

For the design-in of TDA8358J it is advised to use the following design steps:

- **Start with calculating the conversion resistors $R_{CV1,2}$.** Read the typical peak to peak output current $I_{1,2(p-p)}$ and the bias output current $I_{1,2(bias)}$ from the TV signal processor. Take $V_{I(bias)} + V_{I(peak)} < 1.5V$ for room for vertical alignment.(max =1.6V) and take $V_{I(bias)} - V_{I(peak)} > 0.3V$ for optimum linearity

R_{CV} can be calculated by:

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i1,2(bias)} + \frac{I_{i1,2(p-p)}}{2}} \quad \text{or} \quad R_{CV1,2} = \frac{V_{i(bias)} - V_{i(peak)}}{I_{i1,2(bias)} - \frac{I_{i1,2(p-p)}}{2}}$$

When a TDA884X/5X (one chip family), TDA886X/7X/8X (bocma family), TDA935X/6X/8X or TDA955X/6X/8X (ultimate one chip family) TV signal processor is used, a value of **2k2** for $R_{CV1,2}$ will do.

- **Calculate the measuring resistor R_M .** Read the peak to peak value of the vertical deflection current from the picture tube coil specification. This is the edge to edge value, so overscan has to be included (about 5%).

The measuring resistor R_M can be calculated by means of the formula:

$$R_M = \frac{V_{i(dif)(p-p)}}{I_{o(p-p)}}$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB}$$

$$V_{i(dif)(p-p)} = I_{i1(p-p)} * R_{CV1} - (-I_{i2(p-p)} * R_{CV2})$$

- **Calculate the minimum main supply voltage V_P .** It should be as low as possible to avoid high dissipation. Read the DC-resistance $R_{coil(cold)}$ and inductance L_{coil} of the vertical deflection coil. Read the value of V_{loss} in fig 33. Determine the wanted maximum vertical frequency $f_{vert(max)}$.

The required power supply voltage V_P for the first part of the scan:

$$V_{P(1)} = \frac{I_{o(p-p)}}{2} \times (R_{coil(hot)} + R_M) - L_{coil} \times I_{o(p-p)} \times f_{vert(max)} + V_{loss(1)}$$

The required power supply voltage V_P for the second part of the scan:

$$V_{P(2)} = \frac{I_{o(p-p)}}{2} \times (R_{coil(hot)} + R_M) + L_{coil} \times I_{o(p-p)} \times f_{vert(max)} + V_{loss(2)}$$

Eventually, after calculating the voltage supply by means of the above formulae, the minimum required value has to be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. Eventually, this value has to be increased by 5% due to spread in the line output transformer and the deflection coil.

- **Calculate the flyback supply voltage V_{FB} .** Determine the wanted flyback time t_{FB} .
The flyback supply voltage can be calculated by:

$$V_{FB} = \frac{I_{o(p-p)} \times (R_{coil(hot)} + R_M)}{1 - e^{-t_{FB}/x}}$$

Where:

$$x = \frac{L_{coil}}{R_{coil(hot)} + R_M}$$

- **Choose a value of R_s of 2.7k Ω .**
- **Calculate the compensation resistor R_{CMP} .** Take a value of $V_{loss(FB)}$ of 8V. Read the value of the damping resistor R_{D1} . A value of 270 Ω is recommended. Check for damping resistor on the deflection coil unit.

The compensation resistor R_{CMP} is calculated in the following way:

$$R_{CMP} = \frac{(V_{FB} - V_{loss(FB)} - V_P) \times R_{D1} \times (R_S + 300)}{\left(V_{FB} - V_{loss(FB)} - \frac{I_{o(p-p)}}{2} \times R_{coil(hot)} \right) \times R_M}$$

- **Calculate the heatsink.** See sec.2.13 for a detailed description.
- **Check the peak temperature of the junction/die.** See 2.14 for a detailed description.
- **Connect the vertical guard.** See sec. 2.10 for a detailed description.
- **Check that the E - W amplifier is below the SOAR-lines.** At set switch-on or switch off or during adjusting geometry the E - W amplifier may exceed the maximum dissipation. For a repetitive time duration of <0.1 ms the maximum allowed peak dissipation 15W for a non repetitive time duration of <5 ms (set switch-on, set - switch-off) the maximum allowed peak dissipation is also 15W.
- Choose a value of R_{EWF} of 82k between pin 5 INEW and pin 8 OUTEW.
- Good HF decoupling of both supplies (pin 3 and 9) is necessary. The use of a 100 nF foil or MKT capacitor (not SMD) which is mounted as close as possible to both power supply pins and to ground is strongly recommended.
- Recommended values for the elcaps on the supplies are 220 μ F at pin 3 (V_P) and 47 μ F at pin 9 (V_{FB}).
- For flashover or other overstress protection it is recommended to connect an RC-filter between OUTA (pin 10) and VGND (pin 6) that consists of 1.5 Ω in series with 47nF and should be connected as close as possible to the pins of the TDA8358J.

- Pay attention to the symmetry of the tracks to the input pins (pin 1 and 2). Long tracks should be avoided. The use of decoupling capacitors between the input pins and ground minimises the interference susceptibility. Both decoupling capacitors must have the same value and should be placed close to pin 1 and pin 2, just like the input resistors. If the value of these capacitors is too high, minor oscillations *could* occur at the start- or end of the scan. The recommended value is 2.2nF.

3. DIFFERENCES BETWEEN N1 AND N2

In this chapter is given a **summary** of the differences between TDA8358JN1 and TDA8358JN2. **No changes have to be made in the application, when changing from N1 to N2.**

3.1.1 Adaptive control of the flyback switch

The waveform during part B of the flyback waveform has a shape that is created by the adaptive control of the flyback switch, which operates as follows. The output current of the flyback switch is measured on a certain level onwards, the drive of the flyback switch is increased, thus lowering the impedance of the flyback switch at increasing flyback current.

In the TDA8358JN2 the adaptive control circuit is activated at all values of the output current. This results in a lower dissipation in the flyback switch and a somewhat shorter flyback time. In the TDA8358JN1 the adaptive control circuit is not activated at a low output current. The small difference in the output voltage is given in fig 49:

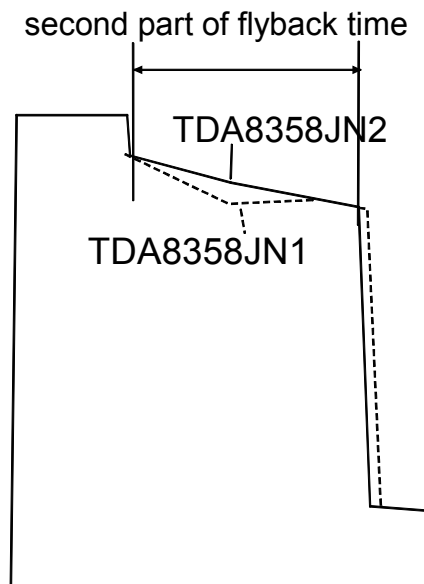


fig 49: Small difference in output voltage (flyback pulse) between N1 and N2

3.1.2 Flashover behaviour of TDA8358JN2

The TDA8358JN2 has improved robustness of the internal low substrate leakage current diodes against flashover by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5Ω) from pin 10 OUTA to pin 6 VGND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during flash testing on critical pins like focus and VG2.

From our experiences with flashover and other overstress testing in the past it is recommended, see fig 50:

- HF decoupling capacitors of the supplies V_P and V_{FB} must be close to pins of the IC in the PCB-layout. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 5 GND. Avoid ground loops in the PCB-layout.

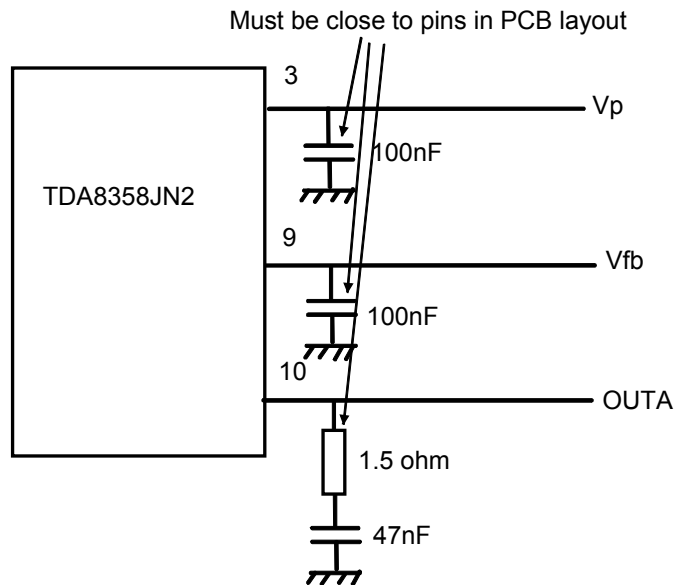


fig 50: Recommended layout for flashover protection

3.2 ESD-gun test

Next to the standard ESD-test on the TDA8358J (Human Body Model and Machine Model), another ESD-test is introduced by some customers. This ESD-test is introduced to test the application, which the TDA8358J is used in. This ESD-test is carried out by a standard ESD-gun (NSG 435), which is discharged on the connections of the vertical deflection coil mounted on the neck of the picture tube. The standard ESD-gun is discharged with a capacity of 150 pF and a series resistor of 330 Ω . This capacitor and resistor are standard IEC1000-4-2 (IEC 801-2, 1991) and are inside of the ESD-gun.

With the TDA8358JN1, some external components were needed for a better ESD-gun test behaviour. The TDA8358JN2 has improved robustness of internal low substrate leakage current diodes against overstress behaviour by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5 Ω) from pin 10 OUTA to pin 6 VGND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during ESD-gun testing up till 16.5 kV air discharge. These values (16.5 kV air discharge and 9kV contact discharge) are the maximum values of the NSG 435 ESD-gun.

From our experiences with ESD-gun testing in the past it is recommended:

- HF decoupling capacitors of the supplies V_P and V_{FB} must be close to pins of the IC in the PCB-layout. When the HF decoupling capacitor of the flyback supply V_{FB} is not close to the pin V_{FB} , the robustness is much lower. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 6 VGND. Avoid ground loops in the PCB-layout.

3.3 Improved temperature coefficient in TDA8358JN2

The TDA8358JN2 has an improved temperature coefficient. A small layout modification is made in the TDA8358JN2, which reduces a temperature influence of the vertical amplitude. This temperature influence is checked in a customer TV-application. The picture height of the picture tube used is 410 mm. The results found are that the temperature influence of the vertical amplitude is reduced by a factor of 2. The behaviour equals our predecessor range of vertical deflection output amplifiers.

4. EXTENDED APPLICATION INVESTIGATION

4.1 Introduction

A more detailed investigation may be required, depending on the application. Whether such an investigation is necessary can be determined by comparing the actual application with the figures in the next sections. However with the TDA8358JN2 such an investigation is not necessary.

4.2 Current peak at the end of flyback time.

For flashover or other overstress protection it is recommended to connect a RC-filter between OUTA (pin 10) and GND (pin 6) that consists of 1.5Ω in series with 47nF and should be connected as close as possible to the pins of the TDA8358J.

When an RC-filter is used between OUTA and GND in an application with the TDA8358J, a small current peak at the end of the flyback time arises. In the next case one can see that these current peaks *don't* damage the TDA8358J.

4.2.1 Application without RC-filter.

In fig 51 the voltage of OUTA (pin 7), the current of OUTA (pin 10) and the current of VGND (pin 6) is measured in an application *without* RC-filter

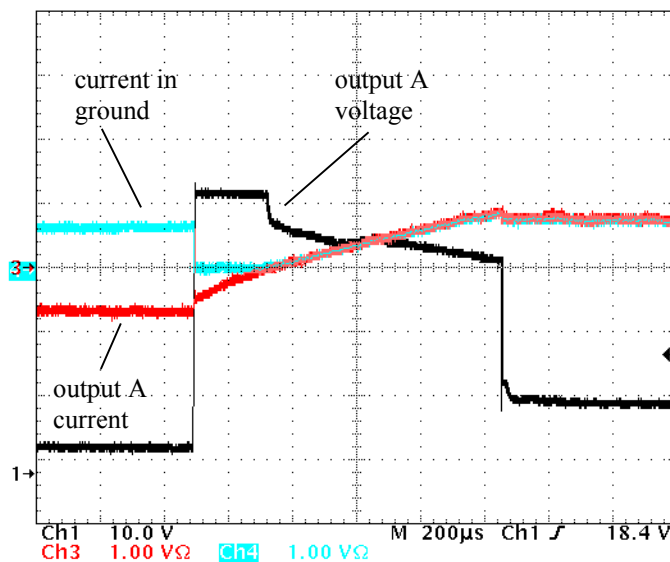


fig 51: Flyback time of application without RC-filter on OUTA

In fig 52 is the beginning of the flyback stretched out and in fig 53 the end of the flyback is stretched out.

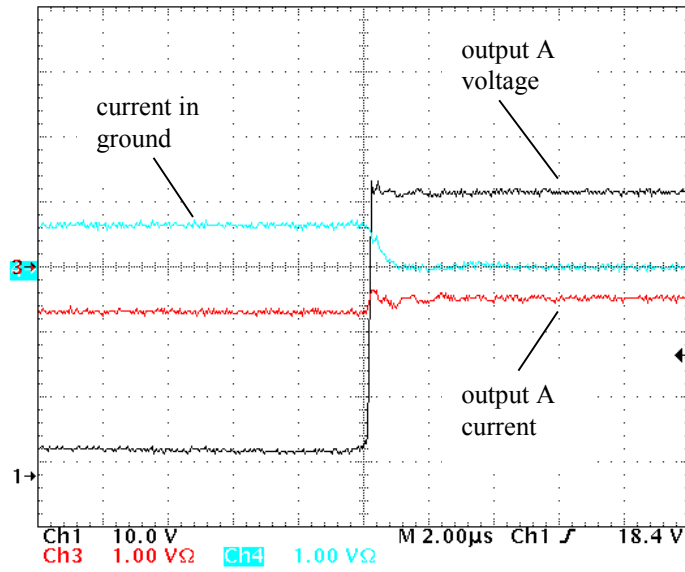


fig 52: Flyback time of application without RC-filter on OUTA.

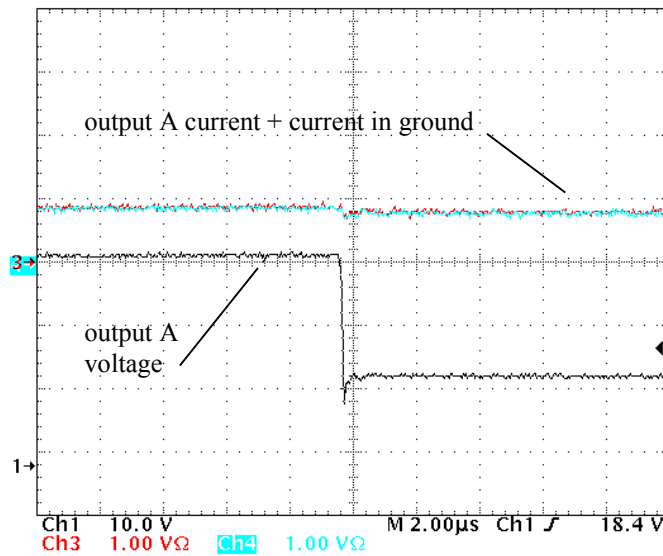


fig 53: Flyback time of application without RC-filter on OUTA.

As can be seen in fig 52 and in fig 53, there are no current peaks at output A or ground at the start- and end of the flyback. The small step in the output A current is the current that flows through the damping resistor.

4.2.2 Application with RC-filter 47 nF + 1.5 Ohm

When a low ohmic RC-filter (47 nF + 1.5 Ohm) is used between OUTA and ground for flash protection, a peak current occurs at OUTA and GND at the end of the flyback. See fig 54 and fig 55.

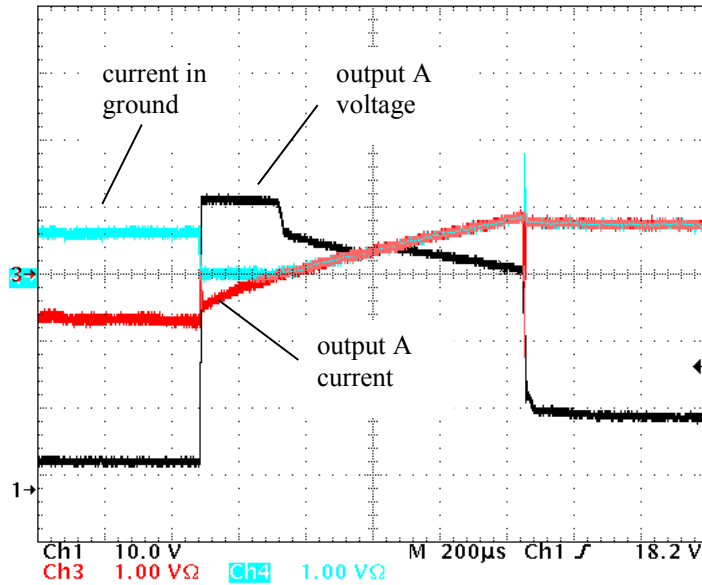


fig 54: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

In fig 55 the beginning of the flyback is stretched out and in fig 56 the end of the flyback is stretched out.

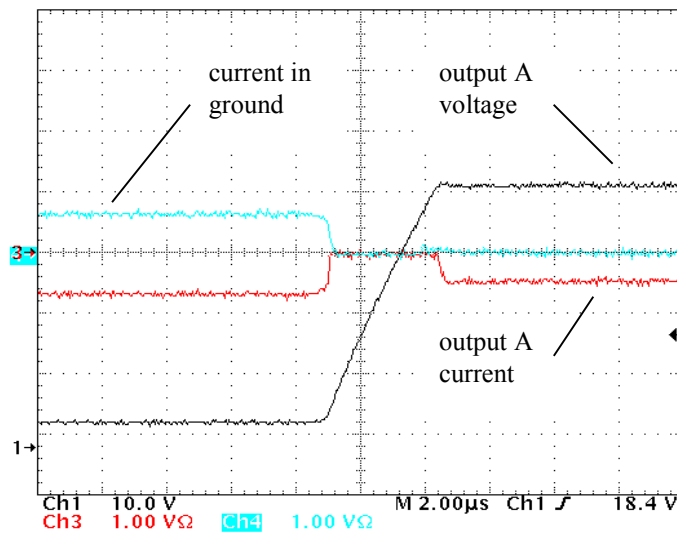


fig 55: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in fig 55 the rise time of the flyback pulse increases when an RC-filter on OUTA is used. This has no influence on the performance of the TDA8358J. During the rise time of the flyback, the current of pin OUTA is zero. This is due to charging the capacitor of the RC-filter. Then the current from the deflection coil flows in the capacitor of the RC-filter.

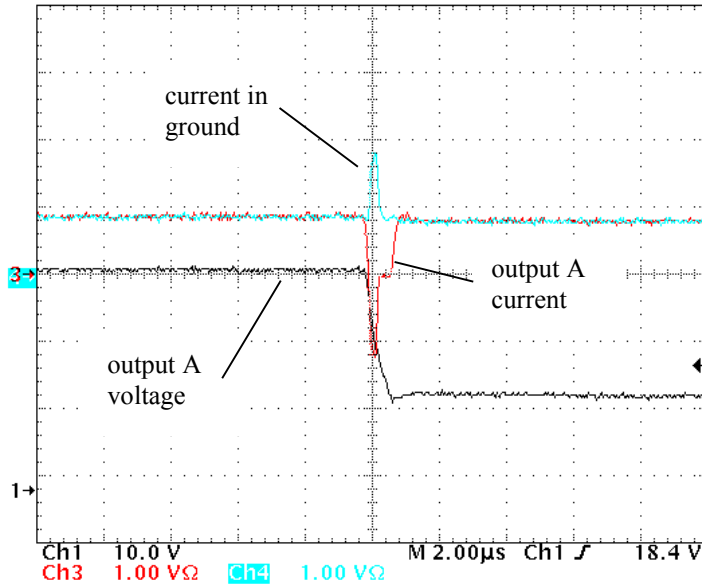


fig 56: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in fig 56 a current peak of 1.8 A occurs in the GND pin at the end of the flyback. Also a negative current peak of 1.2 A occurs in the OUTA at the end of the flyback. These peaks are due to discharge of the capacitor of the RC-filter. The discharge current of the capacitor flows via the bottom transistor of the A-output of TDA8358J to GND. See fig 57. Because the time of these peaks is *very short*, this will cause *no damage* to the TDA8358J.

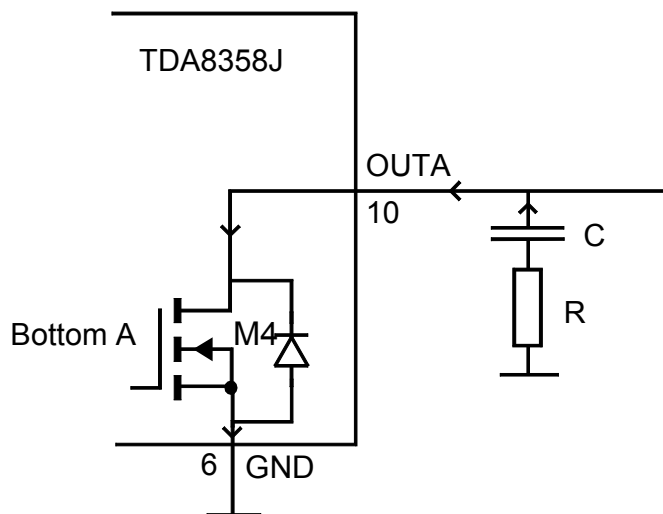


fig 57: TDA8358J, current flow when discharging C.

5. APPENDIX

5.1 Calculating the power P_{sup}

The power that is delivered by the supply is calculated in the following way:

The current (I_{sup}) that is delivered by the power supply during the scan time is illustrated in the figure below.

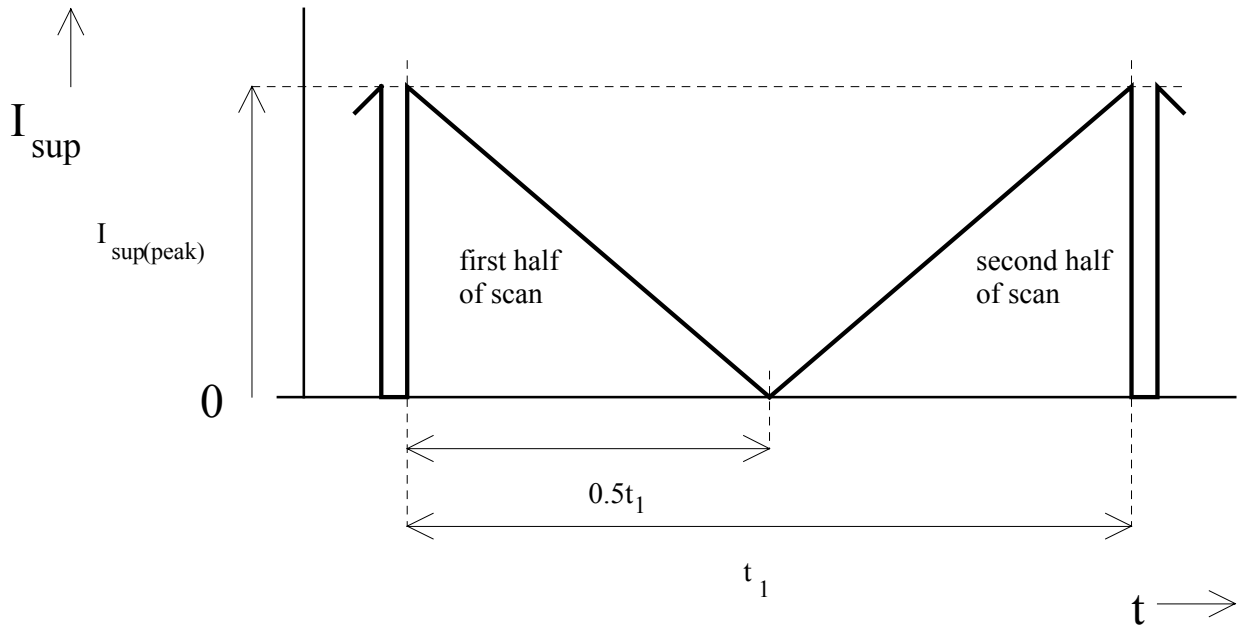


fig 58: Current of the supply.

The *momentary* supply current I_{sup} is expressed by the formula:

$$\text{for } 0 \leq t \leq 0.5t_1 \text{ (first half of the scan):} \quad I_{\text{sup}}(t) = I_{\text{sup(peak)}} - \left(2 \times I_{\text{sup(peak)}} \times \frac{t}{t_1} \right)$$

$$\Leftrightarrow I_{\text{sup}}(t) = I_{\text{sup(peak)}} \times \left(1 - 2 \times \frac{t}{t_1} \right)$$

$$\text{for } 0.5t_1 \leq t \leq t_1 \text{ (second half of the scan):} \quad I_{\text{sup}}(t) = \left(2 \times I_{\text{sup(peak)}} \times \frac{t}{t_1} \right) - I_{\text{sup(peak)}}$$

$$\Leftrightarrow I_{\text{sup}}(t) = I_{\text{sup(peak)}} \times \left(2 \times \frac{t}{t_1} - 1 \right)$$

Because of the symmetry for the first- and the second half of the power supply, the *average* power delivered by the supply is:

$$P_{\text{sup}} = 2 \times \frac{1}{t_1} \times \int_0^{0.5t_1} \left(V_P \times I_{\text{sup}(peak)} - 2 \times V_P \times I_{\text{sup}(peak)} \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\text{sup}} = \frac{2}{t_1} \times \int_0^{0.5t_1} V_P \times I_{\text{sup}(peak)} \times \left(1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\text{sup}} = \frac{2 \times V_P \times I_{\text{sup}(peak)}}{t_1} \times \int_0^{0.5t_1} \left(1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\text{sup}} = \frac{2 \times V_P \times I_{\text{sup}(peak)}}{t_1} \times \left[t - \frac{t^2}{t_1} \right]_0^{0.5t_1}$$

$$\Leftrightarrow P_{\text{sup}} = \frac{2 \times V_P \times I_{\text{sup}(peak)}}{t_1} \times \frac{1}{4} \times t_1$$

$$\Leftrightarrow P_{\text{sup}} = \frac{V_P \times I_{\text{sup}(peak)}}{2}$$

or $P_{\text{sup}} = \frac{V_P \times I_{o(p-p)}}{4}$ because $I_{\text{sup}(peak)} = \frac{I_{o(p-p)}}{2}$

5.2 Calculating the power dissipation P_L

The power dissipation in the load ($R_{coil} + R_M$) is calculated in the following way:

The current through the deflection coil I_o and the current through the measurement resistor R_M are equal and can be seen in fig 59. The influence of the damping resistor R_{D1} (300Ω) can be neglected.

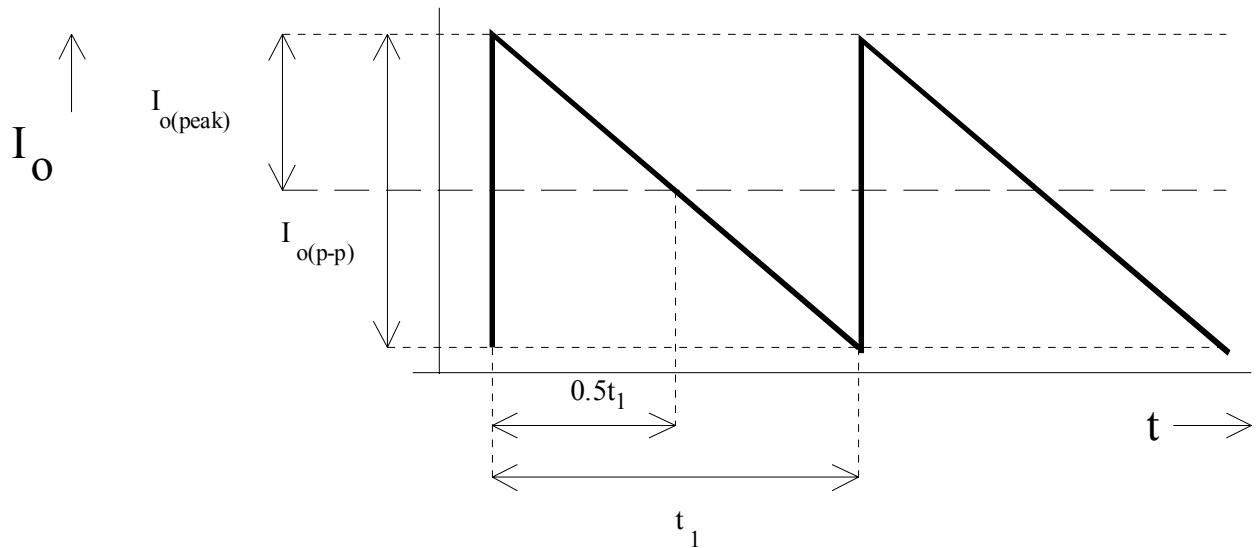


fig 59: Current through the deflection coil and R_M .

The *momentary* current in the deflection coil is given by:

$$I_o(t) = I_{o(peak)} - \left(2 \times I_{o(peak)} \times \frac{t}{t_1} \right)$$

$$\Leftrightarrow I_o(t) = I_{o(peak)} \times \left(1 - 2 \times \frac{t}{t_1} \right)$$

The *momentary* dissipated power $P_L(t)$ in the load ($R_{coil} + R_M$):

$$\text{since: } P = I^2 \times R$$

$$\Leftrightarrow P_L(t) = I_{o(peak)}^2 \times \left(1 - 2 \times \frac{t}{t_1} \right)^2 \times (R_{coil} + R_M)$$

Because of the symmetry of the first- and the second half of the current through the load, the *average* power dissipation in the load is:

$$P_L = \frac{2}{t_1} \times \int_0^{0.5t_1} (I_{o(peak)})^2 \times \left(1 - 2 \times \frac{t}{t_1}\right)^2 \times (R_{coil} + R_M) dt$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{o(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \int_0^{0.5t_1} \left(1 - 2 \times \frac{t}{t_1}\right)^2 dt$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{o(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \int_0^{0.5t_1} \left(1 - 4 \times \frac{t}{t_1} + 4 \frac{t^2}{t_1^2}\right) dt$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{coil(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \left[t - \frac{4}{2} \cdot \frac{t^2}{t_1} + \frac{4}{3} \cdot \frac{t^3}{t_1^2} \right]_0^{0.5t_1}$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{o(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \left[0.5 \cdot t_1 - 2 \cdot \frac{(0.5 \cdot t_1)^2}{t_1} + \frac{4}{3} \cdot \frac{(0.5 \cdot t_1)^3}{t_1^2} \right]$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{o(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \left[\frac{1}{2} \cdot t_1 - \frac{1}{2} \cdot t_1 + \frac{1}{6} \cdot t_1 \right]$$

$$\Leftrightarrow P_L = \frac{2 \times (I_{o(peak)})^2 \times (R_{coil} + R_M)}{t_1} \times \frac{1}{6} \cdot t_1$$

$$\Leftrightarrow P_L = \frac{I_{o(peak)}^2 \times (R_{coil} + R_M)}{3}$$

or $P_L = \frac{I_{o(p-p)}^2 \times (R_{coil} + R_M)}{12}$ because $I_{o(p-p)} = 2 \times I_{o(peak)}$

For calculations the coil resistance is multiplied by 1.2 for hot conditions of the deflection coil

$$P_L = \frac{I_{o(peak)}^2 \times (1.2 \times R_{coil} + R_M)}{3}$$

or

$$P_L = \frac{I_{o(p-p)}^2 \times (1.2 \times R_{coil} + R_M)}{12}$$

6. REFERENCES

- Application note TDA8357JN2 / TDA8359JN2 (AN01056)
- Application note TDA8358JN1 (AN99009)
- Application note TDA935X/6X/8X (AN98093)
- Application note TDA884X/885X (AN98002)

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